SCHOOL
OF
INFORMATION AND COMMUNICATION TECHNOLOGY

COURSE STURCTURE AND DETAILED SYLLABUS

5 YEARS DUAL DEGREE BTECH(ECE)+MTECH/MBA

SPECIALIZATION:

VLSI

GAUTAM BUDDHA UNIVERSITY
GAUTAM BUDH NAGAR, GREATER NOIDA
2011-2012

SEMESTER –I

Sr.No.	Course Code	Courses	L-T-P	Credits
		THEORY		
1	CY101/PH102	Engineering Chemistry/Engineering Physics	3-1-0	4
2	MA101	Mathematics – I	3-1-0	4
3	CE101	Engineering Mechanics	2-1-0	3
4	CS101	Computer Programming – I	2-0-0	2
5	EC101/EE102	Basic Electronics / Electrical Technology	2-0-0	2
6	HU 101	English Proficiency	2-0-0	2
7	SS101	Human Values & Buddhist Ethics	2-0-0	2
		PRACTICALS		
8	CY103/PH104	Engineering Chemistry Lab/Engineering Physics Lab	0-0-2	1
9	CE103	Engineering Graphics Lab	0-0-3	2
10	CS181	Computer Programming Lab –I	0-0-3	2
11	EC181/EE104	Basic Electronics Lab/ Electrical Technology Lab	0-0-2	1
12	GP101	General Proficiency	-	1
		Total	**16-3-10**	**26**
		Total Contact Hours	29	

SEMESTER- II

Sr. No.	Course Code	Courses	L-T-P	Credits
		THEORY		
1	PH102/CY101	Engineering Physics/ Engineering Chemistry	3-1-0	4
2	MA102	Mathematics – II	3-1-0	4
3	CE106	Ecology and Environment	2-1-0	3
4	CS102	Computer Programming – II	2-0-0	2
5	EE102/EC101	Electrical Technology/ Basic Electronics	2-0-0	2
6	HU102	Professional Communication	2-0-0	2
7	SS102	History of Science & Technology	2-0-0	2
		PRACTICALS		
8	PH104/CY103	Engineering Physics Lab/ Engineering Chemistry Lab	0-0-2	1
9	CS182	Computer Programming Lab II	0-0-3	2
10	EE104/EC181	Electrical Technology Lab/ Basic Electronics Lab	0-0-2	1
11	ME102	Workshop Practices	0-0-3	2
12	GP102	General Proficiency	-	1
		Total	**16-3-10**	**26**
		Total Contact Hours	29	

SEMESTER – III

Sr. No.	Course Code	Courses	L-T-P	Credits
		THEORY		
1	MA201	Quantitative Techniques	3-1-0	4
2	EC201/EC431	Digital Electronics	3-0-0	3
3	EC203	Network Analysis and Synthesis	3-0-0	3
4	EC205/EC444	Signal and Systems	2-1-0	3
5	CS205	Data Structures and Algorithms	2-1-0	3
6	EC207	Electronic Devices and Circuits	3-0-0	3
		PRACTICALS		
7	EC281/EC483	Digital Electronics Lab	0-0-3	2
8	CS283	Data Structures and Algorithms Lab	0-0-3	2
9	EC283	Electronic Circuits Lab	0-0-3	2
10	GP201	General Proficiency		1
		Total	**17-2-9**	**26**
		Total Contact Hours	28	

SEMESTER – IV

Sr. No.	Course Code	Courses	L-T-P	Credits
		THEORY		
1	MA202	Numerical Methods of Analysis	3-1-0	4
2	EE202	Measurements and Instrumentation	2-0-0	2
3	EC202	Analog Communication	3-1-0	4
4	EC204	Linear IC Applications	3-0-0	3
5	EC206	Digital Signal Processing	3-0-0	3
6	EC208	Engineering Electromagnetic	3-0-0	3
		PRACTICALS		
7	EE216	Measurements and Instrumentation Lab	0-0-3	2
8	EC282	Analog Communication Lab	0-0-3	2
9	EC284	Digital Signal Processing Lab	0-0-3	2
10	GP202	General Proficiency		1
		Total	**17-2-9**	**26**
		Total Contact Hours	28	

SEMESTER – V

Sr. No.	Course Code	Courses	L-T-P	Credits
		THEORY		
1	EC301	Digital Logic Design	3-0-0	3
2	EC303	Digital Communication Systems	3-0-0	3
3	EC305	Antenna and Wave Propagation	3-1-0	4
4	EE305	Control Theory	3-1-0	4
5	CS309/CS438	Computer Organization and Architecture	3-0-0	3
6	ME311	Principles of Technology Management	2-0-0	2
		PRACTICALS		
7	EC381	Logic Design Lab	0-0-3	2
8	EC383	Digital Communication Lab	0-0-3	2
9	EC385	Antenna and Wave propagation Lab	0-0-3	2
10	GP301	General Proficiency		1
		Total	**17-2-9**	**26**
		Total Contact Hours	28	

SEMESTER – VI

Sr. No.	Course Code	Courses	L-T-P	Credits
		THEORY		
1	EC302	Microwave Engineering	3-1-0	4
2	EC304/EC559	Microprocessors & Interfacing	3-0-0	3
3	EC306/EC446	Microelectronics Engineering	3-0-0	3
4	EC308	Information Theory & Coding	3-1-0	4
5	CS310	Data Networks	3-0-0	3
6	ME312	Entrepreneurship & Innovation	2-0-0	2
		PRACTICALS		
7	EC382	Microwave Engineering Lab	0-0-3	2
8	EC384/EC587	Microprocessor and Interfacing Lab	0-0-3	2
9	CS382	Computer Networks Lab	0-0-3	2
10	GP302	General Proficiency		1
		Total	**17-2-9**	**26**
		Total Contact Hours	28	

SEMESTER – VII

Sr. No.	Course Code	Courses	L-T-P	Credits
		THEORY		
1	SS401	Social Aspects of Engineering	2-1-0	3
2	EC401	Optical Communication	3-0-0	3
3	EC403	Semiconductor Device Modeling and Technology	3-1-0	4
4	EC405	Wireless Mobile Communication	3-1-0	4
5		Elective-1	3-0-0	3
		PRACTICALS		
6	EC481	Optical Communication Lab	0-0-3	2
7	EC491	Seminar	0-0-3	2
8	EC493	Minor Project	0-0-8	4
9	GP401	General Proficiency	-	1
		Total	**14-3-14**	**26**
		Total Contact Hours	31	

Elective-1

Sr.No	Course Code	Courses
1	EC441	Design with Microcontrollers
2	EC443	Telecommunication Switching and Networks
3	EC445	Satellite Communication
4	EC447	Digital Image Processing
5	EC449	Communication Networks and Transmission Lines
6	EC465/EC555	Principles of VLSI Design
7	EC467	RADAR and TV Engineering
8	CS441/CS541	Software Project Management
9	CS443/CS543	Object Oriented Software Engineering

SEMESTER- VIII

Sr. No.	Course Code	Courses	L-T-P	Credits
		THEORY		
1	MA402	Simulation and Modeling	3-1-0	4
2	EC410/EC536	VLSI Technology	3-0-0	3
3	EC440/EC538	Advanced Analog VLSI Design	3-0-0	3
4		Elective-3	3-0-0	3
5		Elective-4	3-0-0	3
		PRACTICALS		
6	EC484/EC560	Design Lab II	0-0-3	2
7	EC492/EC592	Major Project	0-0-10	5
8	GP402	General Proficiency	---	1
		Total	**15-1-13**	**24**
		Total Contact Hours	29	

Electives (3 & 4)

Sr.No	Course Code	Courses
1.	EC408/EC566	VLSI for Wireless Communication
2.	EC406/EC542	Quality of Services in Networks
3.	CS447/CS547	Multimedia Techniques
4.	CS449/CS561	Soft Computing
5.	EC404/EC534	Wireless System Design
6.	CS404/CS534	Open Source Software System
7.	EC430/EC568	Design of Semiconductor Memories
8.	EC422/EC570	Principles of MEMS Design
9.	EC432/EC572	Solid State Electronics Devices
10.	EC434/EC574	Integrated Circuit Physical Design
11.	EC428/EC576	CMOS RF Circuit Design
12.	EC436/EC578	CMOS VLSI Design
13.	EC438/EC580	VLSI Design Techniques
14.	EC412/EC544	Advanced RF Engineering
15.	EC424/EC548	Probability and Stochastic Processes
16.	EC426/EC550	Advanced Microwave Communication
17.	EC418/EC556	Image Processing and Biometrics
18.	EC402/EC532	Advanced Communication Networks

SUMMER SEMESTER (After 8th Semester)

Sr. No.	Course Code	Courses	L-T-P	Credits
1	EC490	Project	0-0-20	10
		Total	0-0-20	**10**
		Total Contact Hours	20	

SEMESTER – IX

Sr. No.	Course Code	Courses	L-T-P	Credits
		THEORY		
1	EC503/EC633	Low Power VLSI Design	3-0-0	3
2	CS503/CS633	Research Techniques in ICT	3-0-0	3
3		Elective- 5	3-0-0	3
4		Elective- 6	3-0-0	3
		PRACTICALS		
5	EC583/EC683	Design Lab III	0-0-3	2
6	EC591/EC691	Dissertation Part-I	0-0-14	7
7	GP501	General Proficiency	---	1
		Total	**12-0-17**	**22**
		Total Contact Hours	29	

Electives (5 & 6)

Sr.No	Course Code	Courses
1.	EC523/EC665	VLSI ASIC Design
2.	EC525/EC667	Micro and Smart System Technology
3.	EC527/EC669	Advances in VLSI Design
4.	EC517/EC671	Modern Optimization Techniques
5.	EC529/EC673	VLSI-Reliability Engineering
6.	EC511/EC647	Sensor Network
7.	EC519/EC675	Mixed-Signal VLSI Design
8.	EC521/EC677	DSP Integrated Circuits
9.	EC545/EC679	Advanced Digital VLSI Design
10.	EC547/EC659	Test and Verification of VLSI Circuits
11.	EC549/EC661	EM Interference and Capabilities in System Design
12.	EC551/EC663	Algorithm for VLSI Design Automation
13.	EC507/EC643	Smart Antenna System

Semester -X

Sr. No	Course Code	Courses	L-T-P	Credits
1	EC590/EC690	Dissertation Part-II	---	21
2	GP502	General Proficiency	---	1
		Total	**---**	**22**

Grand Total Credits = 260

BASIC ELECTRONICS			
Course Code:	**EC101**	**Credits:**	**2**
No. of Lectures (Hrs/Week):	**2**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**30**	**End Sem Exam Hours:**	**3**

Unit I:

Passive Components

Resistances, Capacitors and Inductors, Component Specifications, Applications, Response to dc and sinusoidal voltage/current excitations

Semiconductor Theory

Metals, Insulators and Semiconductor materials, energy band diagram, Intrinsic and Extrinsic Semiconductors, Doping, Fermi level, Fermi level of P-type and N-type materials, Mobility, Drift Current and Diffusion Current. Current conduction in Semiconductors, Generation and Recombination of Charges

Unit II: Semiconductor Diodes

Theory of P-N Junction, Ideal & Practical diode, Concept of AC and DC Resistances, V-I Characteristics, Diode Equivalent Circuits, Transition and Diffusion Capacitance, Reverse Recovery Time, Zener and Avalanche breakdown, Tunnel Diodes, Varactor Diode, Light Emitting Diode

Unit III: Diode Applications and Wave Shaping Circuits

Load line analysis, series and parallel combinations, Half wave & Full wave Rectifiers, Clippers & Clampers.

Unit IV: Transistors

Bipolar Junction Transistor- Construction, Operation, Transistor Configurations, Input and Output Characteristics, AC and DC Load line, operating point, Effect of shifting the operating point. Biasing, Thermal Runaway, Effect of temperature on the characteristics, Early effect, introduction to JFET and MOSFET

Unit V: Logic Gates and Operational Amplifiers

Binary number, Digital systems, Boolean algebra, logic gates, logic functions, realization of logic gates by electronic devices, Positive and negative logic, representation of binary numbers, half adder, full adder, flip-flops, Op-Amp, Practical Op-Amp, Open loop and closed loop configurations, Applications of Op-Amps as inverting and non-inverting amplifier

Text Books:

[1] Boyelasted an Nashlsky: Electronics Devices and circuit Theory, TMH.
[2] Gayakwad :Op-Amps and Linear Inegrated Circuits , PHI.

References:

[1] Millman & Halkias :Integrated Electronics ,TMH.
[2] Morris Mano: Digital Design ,PHI.
[3] Malvino :Electronics Principles,TMH.

COMPUTER PROGRAMMING-I LAB			
Course Code:	**CS182**	**Credits:**	**2**
No. of Practical (Hrs/Week):	**3**		
Total No. of Lab Sessions:	**10**	**End Sem. Exam Hours:**	**2**

Programs/Experiments List:

1. Write a C program to reverse a given number, find the sum of digits of the number.
2. Write a C program to concatenate two strings.
3. Write a C program to take marks of a student as input and print the his/her grade bases on following criteria using if – else statements

Marks <40	FAIL
40<= Marks <59	GOOD
59 <= Marks < 80	Excellent
80 <= Marks	Outstanding

4. Perform experiment 3 using switch case statement.
5. Write a C program to compute the length of a string using while loop.
6. Write a C program to convert all the lowercase letter to uppercase letter and all uppercase letters to lower case letter given a string as input.
7. Write a C program to compute the roots of a quadratic equation.
8. Write a C program to check whether a given number is prime or not, also check whether it is divisible by a number k or not.
9. Write a C program to check whether a given year is leap year or not.
10. Write a C program to take two matrixes as input and print the sum of two matrixes.
11. Write a C program to display the address of a variable using pointer.
12. Write a C program to compute the length of a string using pointer.
13. Create a structure called STUDENT having name, registration number, class, session as its field. Compute the size of structure STUDENT.
14. Write a C program to check weather a given string is palindrome or not.
15. Write a C program to generate following patterns.

```
        1
      2   2
    3   3   3
  4   4   4   4
```

```
        A
      B   B
    C   C   C
  D   D   D   D
```

BASIC ELECTRONICS LAB			
Course Code:	**EC181**	**Credits:**	**1**
No. of Lab (Hrs/Week):	**2**	**End Sem Exam Hours:**	**3**
Total No. of Lab Sessions:	**10**		

List of Experiments

1. Study of Multimeter and Function Generator /Counter.
2. Study of Cathode-Ray Oscilloscope.
3. To calculate the Equivalent Resistance of the Series and parallel resistive network.
4. To calculate the Equivalent Capacitance of the Series and parallel capacitive network.
5. To Plot the V-I Characteristics of P-N Junction Diode in forward bias and reverse bias.
6. To study the working of a P-N Junction Diode as a switch.
7. To plot the V-I Characteristics of a Zener Diode.
8. To plot the input and output waveforms of clipper circuits.
9. Study the Half wave rectifier.
10. Study of Full wave Bridge Rectifier.
11. Study of Centre Tapped Full Wave Rectifier.
12. To plot the input and output characteristic of transistor's Common Base configuration.
13. To plot the input and output characteristic of transistor's Common Emitter configuration.
14. To plot the input and output characteristic of transistor's Common Collector configuration.
15. To verify the truth table of various logic gates.

COMPUTER PROGRAMMING-II LAB			
Course Code:	**CS182**	**Credits:**	**2**
No. of Practical (Hrs/Week):	**3**		
Total No. of Lab Sessions:	**10**	**End Sem. Exam Hours:**	**2**

Programs/Experiments List:

1. Write a separate Java Code to implement each of the following:

   Class, Command Line Argument, how to enter value through keyboard

2. Write a separate Java Code to implement each of the following data types:

   Variable, Constant, Arrays, Strings, Vectors, Wrappers Classes, Type Casting

3. Write a separate Java Code to implement each of the following operators:

   Arithmetic operator, Relational operator, Logical operator, Assignment operator, Increment & Decrement operator, Conditional operator, Bitwise operator, ?: operator

4. Write a separate Java Code to implement each of the following control statements:

   Decision statement, Loops statement and Branch statements

5. Write a separate Java Code to implement each of the following sorting:

   Bubble Sort, Selection Sort, Insertion Sort, Merge Sort

6. Write a separate Java Code to implement each of the following:

   Class, Object, Constructors, Method, Method Overloading and Method Overriding

7. Write a separate Java Code to implement each of the following:

   Final variable, final class, final method, abstract class, abstract method and concrete method

8. Write a separate Java Code to implement each of the following OOPs concepts:

   Abstraction, Polymorphism, Encapsulation, Inheritance

9. Write a separate Java Code to implement each of the following:

   Exception handling with Try, Catch, Throw, Throws, Finally

   Multiple catch statement with the following exceptions :

   ArithmeticException, ArrayOutOfBoundsException and ArrayStoreException

10. Write a separate Java Code to implement each of the following:

    Visibility Controls: Private, Public and Protected

11. Write a separate Java Code to implement each of the following:

    Interface, extending and implementing interface

12. Write a separate Java Code to implement each of the following:

    Multithreading: Create thread with thread class and runnable interface, thread priorities, synchronization

13. Write a separate Java Code to implement each of the following:

Packages : Create package A with following methods and import this package A into another Java program to show the result of methods of package A.

i)	First method:	Factorial number with the help of recursion.
ii)	Second method:	Fibonacci Series
iii)	Third Method:	Generate first 10 prime numbers and show the sum of first 10 prime numbers.

14. Write Java Code to generate the following output on applet with the help of two dimensional array and show the result with the help of HTML file.

7 14 21 28 35 42 49 56 63 70	Sum = 385
5 10 15 20 25 30 35 40 45 50	Sum = 275
3 6 9 12 15 18 21 24 27 30	Sum = 165

15. Write a Java Code to design the following web page with the help of applet and HTML.

School of Information and Communication Technology
GAUTAM BUDDHA UNIVERSITY
GREATER NOIDA

- **Student Name:**
- **Enrollment Number:**
- **Programme Name:**
- **Semester:**
- **Course Name:**
- **E-Mail ID:**
- **Mobile Number:**
- **Blood Group:**

DIGITAL ELECTRONICS LAB			
Course Code:	**EC483/EC281**	**Credits:**	**2**
No. of Lab (Hrs/Week):	**3**	**End Sem Exam Hours:**	**3**
Total No. of Lab Sessions:	**10**		

List of Experiments

1. Verify the truth table of AND Gate
2. Verify the truth table of OR and NOT gates.
3. Verify the truth table of NAND , NOR Gates.
4. Verify the truth table of and EX-OR Gate.
5. Design a combinational circuit to realize the function f(ABC)=A(B+C) using NAND gates only.
6. Design a half adder using NOR gates only
7. Design full adder
8. Design a given size of Mux using gates.
9. Verify RS and JK flip flops
10. Verify D and T Flip flops
11. Design a up/down 3-bit counter
12. Design a 3 bit shift register.

DIGITAL ELECTRONICS			
Course Code:	**EC201/EC431**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exams Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exams Hours:**	**3**

Unit I: Review of Number systems and Binary codes, Binary arithmetic: addition, subtraction, multiplication and division algorithms. Boolean algebra: theorems and functions, Simplification of Boolean functions, minimization techniques, Karnaugh's map method,Quine and McCluskey's method, realization of various binary functions using AND ,OR,NOT,XOR logic gates.

Unit II: Universal gates: NAND, NOR, realization of boolean function using universal gates. Half and full adder, half and full subtractor, Series and parallel adder, BCD adders, look-ahead Carry adder. Decoders, Encoders, multiplexers and de-multiplexers. Analysis and design of combination circuits, realization of various Boolean functions using NAND,NOR gates and multiplexers.

Unit III: Flip-Flops: R-S, Clocked R-S, T, D, J-K, race around problem, Master-slave J-K., State and Excitation Tables, Multivibrators- Astable, Monostable and bistable multivibrators, 555 timer chip and its application in multivibrators

Unit IV: Shift registers and counters, synchronous and asynchronous counters, Binary ripple counter, up-down counter, Johnson and ring counter, Analysis and Design of Sequential Circuits, SISO, SIPO, PISO, PIPO soft registers.

Unit V: Logic families: RTL, DTL, TTL, ECL, IIL, PMOS, NMOS and CMOS logic

Text Books:

[1] M. Mano :Digital Logic and Computer Design, Pearson Education
[2] William I. Fletcher :An Engineering Approach to Digital Design, Pearson Education
[3] R.P. Jain: Digital Electronics, TMH

References:

[1] M. Mano : Digital Design, Pearson Education
[2] W.H. Gothman : Digital Electronics, PHI.
[3] Millman and Taub : Pulse, Digital and Switching Waveforms, MGH
[4] Anand Kumar : Pulse and Digital Circuits , PHI
[5] Leach and Malvino : Digital Principles and Applications, TMH

NETWORK ANALYSIS AND SYNTHESIS			
Course Code:	**EC203**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: Introduction to Circuits
Voltage, Ideal Voltage Source, Current Ideal Current Sources, Classification of Circuits, Ohm's Law, Resistively, Temperature Effect, Resistors, Resistor Power Absorption, Nominal Values and Tolerances, Color Codes, Open and Short Circuits, Internal Resistance. Operational Amplifiers, Capacitance, Inductance, Transformers.

Unit II: Network Theorems for DC applications
DC Circuits: Series and Parallel Circuits, Kirchhoff's Voltage and Current Law, Mesh Analysis, Loop Analysis, Nodal Analysis, Thevenin's and Norton's Theorem, Maximum Power Transfer Theorem, Superposition Theorem, Millman's Theorem, Tellegen's Theorem, Star - Delta and Delta -Star Transformation, Bridge Circuits.

Unit III: Network Theorems for AC applications
AC Circuits: Circuits containing Capacitors and Inductors, Transient Response, Alternating Current and Voltages, Phasors, Impedences and Admittance, Mesh Analysis, Loop Analysis, Nodal Analysis, Thevenin's and Norton's Theorem, Star-Delta and Delta-Star Transformation, Bridge Circuits. Resonant Circuits, Complex Frequency and Network Function, Maximum Power Transfer Theorem, Superposition Theorem.

Unit IV: Network Function and Two port Networks
Network function & Two port networks – concept of complex frequency, Network & Transfer functions for one port & two ports, poles and zeros, Necessary condition for driving point & transfer function. Two port parameters – Z,Y, ABCD, Hybrid parameters, their inverse & image parameters, relationship between parameters, Interconnection of two ports networks, Terminated two port network.

Unit V: Network Synthesis
Hurwitz polynomials, positive real functions. Properties of real immittance functions, synthesis of LC driving point immittances, properties of RC driving point impedances, synthesis of RC impedances or RL admittances, properties of RL impedances and RC admittances.

Text Books:
[1] Decarlo Lin: Linear circuit Analysis; Oxford
[2] Franklin F. Kuo : Network Analysis and synthesis, 2nd Edition, Wiley India Pvt Ltd.

References:
[1] M.E. Van Valkenburg :Network Analysis, (PHI).
[2] Chakraborti :Circuit theory, Dhanpat Rai.
[3] Sudhakar Shyam Mohan: Network Analysis and Synthesis

SIGNAL AND SYSTEMS			
Course Code:	**EC205/EC444**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: LTI Systems

Classification of signals continuous time and discrete time signals, Even and Odd signals, Elementary continuous time and discrete time signals, Classification of systems, causality; stability, time invariance, linearity, Continuous time and Discrete time LTI Systems, convolution Integral and convolution sum, Properties of LTI Systems, Differential and Difference equations. Singularity functions.

Unit II: Analysis of Periodic Signals

Fourier series representation of CTFS, convergence of FS, Properties of CTFS, Fourier series representation of DTFS. Fourier series and LTI Systems, Filtering, RC low pass and high pass filters. Recursive and Non recursive Discrete Time filters, Sampling theorem, sampling of continuous time signal with impulse train and zero order hold Reconstruction, Aliasing, Discrete-time processing of continuous time signals, Digital differentiator, Sampling of discrete time signals, decimation and Interpolation

Unit III: Analysis of Aperiodic Signals

Continuous Time Fourier Transform (CTFT), Convergence of FT. Properties of CTFT, Discrete time Fourier Transform (DTFT), Properties of DTFT. System characterized by linear constant co-efficient differential equations. Magnitude and phase spectrum, group delay, Time domain and frequency domain aspects of ideal Non-ideal filters. First order and second order continuous time and discrete time systems

Unit IV: Laplace Transform

The Laplace transform, Region of convergence, Inverse Laplace transform. Geometric evaluation of Fourier transform from pole zero plot, First order, second order and all pass systems. Properties of Laplace transform Analysis and characterization of LTI systems using the Laplace transform. Causality, stability, Differential equations, Butterworth and Chebychev filters. Unilateral Laplace transform its properties and uses.

Unit V: Convolution and Correlation of Signals

concept of convolution in time domain and frequency domain, graphical representation of convolution, convolution property of Fourier Transform, cross-correlation and auto-correlation of functions, properties of correlation function, energy density spectrum, Parseval's Theorem, power density spectrum, detection of periodic signals in the presence of noise by correlation

Text Books:

[1] Oppenheim Willsky and Nawab,:Signals and Systems, PHI.
[2] Simon Haykin: Signals and Systems, John Wiley.

Reference Books:

[1] Taub and Schilling: Principles of Communication Systems, TMH.
[2] Dungan F R: Electronic Communication Systems, Thomas-Delmar.

DATA STRUCTURES AND ALGORITHMS			
Course Code:	**CS205/CS434**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**2+1T**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**30**	**End Sem Exam Hours:**	**3**

Unit I: Introduction: Basic Terminology, Elementary Data Organization, Algorithm, Efficiency of an Algorithm, Time and Space Complexity, Asymptotic notations: Big-Oh, Time-Space trade-off.
Arrays: Definition, Single and Multidimensional Arrays, Representation of Arrays: Row Major Order, and Column Major Order, Application of arrays, Sparse Matrices and their representations.
Linked lists: Array Implementation and Dynamic Implementation of Singly Linked Lists, Doubly Linked List, Circularly Linked List, Operations on a Linked List. Insertion, Deletion, Traversal, Polynomial Representation and Addition, Generalized Linked List
.
Unit II: Stacks: Abstract Data Type, Primitive Stack operations: Push & Pop, Array and Linked Implementation of Stack in C, Application of stack: Prefix and Postfix Expressions, Evaluation of postfix expression, Recursion, Tower of Hanoi Problem, Simulating Recursion, Principles of recursion, Tail recursion, Removal of recursion
Queues: Operations on Queue: Create, Add, Delete, Full and Empty, Circular queues, Array and linked implementation of queues in C, Dequeue and Priority Queue.

Unit III: Trees: Basic terminology, Binary Trees, Binary Tree Representation: Array Representation and Dynamic Representation, Complete Binary Tree, Algebraic Expressions, Extended Binary Trees, Array and Linked Representation of Binary trees, Tree Traversal algorithms: Inorder, Preorder and Postorder, Threaded Binary trees, Traversing Threaded Binary trees, Huffman algorithm.
Search Trees: Binary Search Trees(BST), Insertion and Deletion in BST, Complexity of Search Algorithm, AVL trees, Introduction to m-way Search Trees, B Trees & B+ Trees

Unit IV: Graphs: Terminology, Sequential and linked Representations of Graphs: Adjacency Matrices, Adjacency List, Graph Traversal : Depth First Search and Breadth First Search, Connected Component, Spanning Trees, Minimum Cost Spanning Trees: Prims and Kruskal algorithm. Transistive Closure and Shortest Path algorithm: Warshal Algorithm and Dijikstra Algorithm.

Unit V: Searching: Sequential search, Binary Search, Comparison and Analysis Internal Sorting: Insertion Sort, Selection, Bubble Sort, Quick Sort, Two Way Merge Sort, Heap Sort, Radix Sort, Practical consideration for Internal Sorting.
Hashing: Hash Function, Collision Resolution Strategies Storage Management: Garbage Collection and Compaction.

Text books:

[1] Aaron M. Tenenbaum, Yedidyah Langsam and Moshe J. Augenstein :Data Structures Using C and C++ , PHI
[2] R. Kruse etal: Data Structures and Program Design in C, Pearson Education
[3] Lipschutz: Data Structures, Schaum's Outline Series, TMH

References Books:

[1] Horowitz and Sahani: Fundamentals of Data Structures", Galgotia Publication
[2] Jean Paul Trembley and Paul G. Sorenson: An Introduction to Data Structures with applications, McGraw Hill

ELECTRONIC DEVICES AND CIRCUITS			
Course Code:	**EC207**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: Review: p-n junction diode, spice model, diode as a switch, BJT-parameters, transistor biasing and stabilization, biasing circuits-analysis and design, equivalent circuits, DC model, h-parameters model, r_e model and hybrid π model, spice model, single stage RC coupled amplifier-load line, gain bandwidth product, emitter follower, BJT as a switch, Power amplifiers

Unit II: JFET: Structure, operating principle, amplifier, biasing analysis, small signal model of JFET, MOSFET-enhancement and depletion type, I-V characteristics, MOSFET amplifiers, introduction to SCR and UJT

Unit III: Multistage BJT amplifiers: classification, distortion, frequency response, RC-coupled amplifier and its low frequency response, high frequency response of an RC-coupled amplifier, multistage CE amplifier cascade at high frequency, Tuned amplifiers-single tuned, double tuned, and staggered tuned amplifiers

Unit IV: Feedback Amplifier: Concept of feedback, classification, transfer gain, general characteristics, effect of feedback on input and output characteristics, analysis of feedback amplifier, voltage series feedback, current series feedback, current shunt feedback, voltage shunt feedback

Unit V: Oscillators: Positive feedback amplifier, Barkhausen Criterion, sinusoidal oscillators, phase shift oscillator, resonant circuit oscillator, general form of oscillator circuit, crystal oscillator, regulated power supplies, series regulators, three terminal IC regulators, switched mode power supplies

Text Books:

[1] J.Millman, C.C.Halkias, and Satyabratha Jit : Electronic Devices and Circuits ,Tata McGraw Hill, 2nd Ed., 2007.
[2] R.L. Boylestad and Louis Nashelsky :Electronic Devices and Circuits , Pearson/Prentice Hall,9th Edition,2006.

References:

[1] T.F. Bogart Jr., J.S.Beasley and G.Rico: Electronic Devices and Circuits, Pearson Education.
[2] S.G.Burns and P.R.Bond: Principles of Electronic Circuits, Galgotia Publications.
[3] Millman and Grabel: Microelectronics, Tata McGraw Hill.
[4] David Bell: Electronic Devices and Circuits, TMH

ELECTRONICS CIRCUITS LAB			
Course Code:	**EC283**	**Credits:**	**2**
No. of Lab (Hrs/Week):	**3**	**End Sem Exam Hours:**	**3**
Total No. of Lab Sessions:	**10**		

List of Experiments

1. To study the switching action of a transistor as a switch.
2. To calculate the h-parameter of transistor in CE mode.
3. To draw the input and output waveforms of power amplifier.
4. To draw the input and output waveforms of single stage R-C coupled amplifier.
5. To draw the input & output characteristics of JFET.
6. To draw the input & output characteristics of MOSFET.
7. To study the transistor as an amplifier in CE mode.
8. To study the transistor as an amplifier in CC mode.
9. To plot the characteristics of SCR.
10. To plot the characteristics of UJT.
11. To study of OP-amp as inverting amplifier.
12. To study of OP-amp as non- inverting amplifier.
13. To study the Hartley oscillator.
14. To study the Phase –Shift oscillator.
15. To study the Wien Bridge oscillator.

DATA STRUCTURES AND ALGORITHMS LAB			
Course Code:	**CS283**	**Credits:**	**2**
No. of Lab (Hrs/Week):	**3**	**End Sem Exam Hours:**	**3**
Total No. of Lab Sessions:	**10**		

List of Experiments

1. Run time analysis of Fibonacci Series
2. Study and Application of various data Structure
3. Study and Implementation of Array Based Program
    a. Searching (Linear Search, Binary Search)
    b. Sorting (Bubble, Insertion, Selection, Quick, Merge etc)
    c. Merging
4. Implementation of Link List
    a. Creation of Singly link list, Doubly Linked list
    b. Concatenation of Link list
    c. Insertion and Deletion of node in link list
    d. Splitting the link list into two link list
5. Implementation of STACK and QUEUE with the help of
    a. Array
    b. Link List
6. Implementation of Binary Tree, Binary Search Tree, Height Balance Tree
7. Write a program to simulate various traversing Technique
8. Representation and Implementation of Graph
    a. Depth First Search
    b. Breadth First Search
    c. Prims Algorthim
    d. Kruskal's Algorithms
9. Implementation of Hash Table

ANALOG COMMUNICATION			
Course Code:	**EC202**	**Credits:**	**4**
No. of Lectures (Hrs/Week):	**3+1 T**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: Spectral Analysis: overview of Fourier Series and Fourier Transform, their Properties, Transform of Gate Signal, Impulse Function and Unit Step Function, Fourier Transform Technique for Periodic Signal, Transform of Train of Pulses and Impulses, Sine and Cosine wave. Signal Energy and Power, Spectral Density of various types of signals, Spectra (Parseval's Theorem), Density Spectra of Periodic Gate. Linear Time Invariant (LTI) Systems, Impulse Response, Convolution, Convolution with Impulse Function, Casual and Non Causal System, Distortion less System, Conditions for Distortion less Transmission. Ideal Filters and Practical Filters

Unit II: Modulation Techniques: Need and types of modulation techniques, Amplitude Modulation, Frequency Spectrum, Power Distribution, AM Modulators, Suppressed Carrier Generation-Balance/Chopper and Square Law Modulation, SSB Generator-Phase and Frequency Discrimination Method, VSB Transmission and Application. Detection of AM signals: Envelope Detector Circuit, RC Time Constant, Synchronous Detection Technique, SSB signal detection, PLL, FDM

Unit III: Angle Modulation: Frequency and Phase Modulation, Frequency spectrum, Bandwidth requirement, Frequency and Phase Deviation, Modulation Index, Narrowband FM, Wide Band FM & their Spectrum . FM Modulators: Direct and Indirect Methods of frequency modulation. FM Detector: Slope Detector, Foster-Seely Discriminator, Ratio Detector, PLL detectors, Pre-Emphasis & De-Emphasis, Capture Effect

Unit IV :AM Transmitter Block Diagram, TRF Receiver & Its Limitations, Necessity of Heterodyning, Super Heterodyne Radio Receivers, IF Amplifiers & Selection of Intermediate Frequency, FM Transmitters, FM Receivers, AGC, AVC, AFC, Dynamic Range of Receivers

Unit V: Classifications of noise, sources of noise, methods of noise calculation in networks, addition of noise due to several sources, noise voltage, noise temperature, noise figure-its calculation and measurement, mathematical representation of random noise, signal to noise ratio, noise bandwidth,

Text Books:

[1] Lathi B.P.: Analog and Digital Communication systems, 3/E Oxford Press, 2007
[2] Kennedy Davis "Electronic Communication Systems" Tata McGraw
[3] Haykin Simon: Communication Systems,4/E John Willey & Sons, 2006.

Reference Books:

[1] Singh R.P. & Sapre: Communication systems Analog & Digital, 2/E TMH, 2007
[2] Bruce Carlson: Communication Systems, 5/E McGraw Hill, 2004.
[3] Proakis and Salehi: Fundamentals of Communication Systems, 1/E Pearson Education, 2005.
[4] Hwei P Hsu: Analog and Digital Communication Schaum Series TMH, 2 Edition.
[5] Taub & Schilling: Principles of communication systems, 3/E McGraw Hill, 2000.

LINEAR IC APPLICATIONS			
Course Code:	**EC204**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: Differential and Cascade Amplifier
Balanced, unbalanced output differential amplifiers, FET differential amplifier, current mirrors, level Translators, cascade configuration of amplifier, operational amplifiers, Introduction to ideal OP-AMP, characteristic parameters, Interpretation of data sheets, Practical OP-AMP, its equivalent circuit and op-amp circuit configuration.

Unit II: Op-Amp with Negative Feedback and Frequency Response
Block diagram representation of feedback amplifier, voltage series feedback, voltage shunt feedback differential amplifier, frequency response compensating network, frequency response of internally compensative op-amp and non compensating op-amp. High frequency op-amp equivalent circuit, open loop gain Vs frequency, closed loop frequency response, circuit stability, and slew rate.

Unit III: Op-Amp Applications
DC, AC amplifier, peaking amplifier, summing ,stealing ,averaging and instrumentation amplifier differential input amplifier, voltage to current converter, current to voltage converter, very high input impedance circuit, integration and differential circuit, wave shaping circuit, active filters, oscillators.

UNIT IV: Linear IC Applications
Log–Anti Log Amplifiers, Multiplier and divider. Precision Rectifiers, Peak Detectors, Sample and Hold Circuits, Analog Multipliers and their applications. Op-amp as a comparator, Zero crossing detector, Schmitt Trigger, Astable multi-vibrator, Mono-stable multi-vibrator, Generation of Triangular Waveforms

Unit V: Data Converters and PLL
A/D and D/A converters. Phase locked loop, Ex-OR Gates and multipliers as phase detectors, Block Diagram of IC PLL, Working of PLL and Applications of PLL.

Text Books:
[1] R.A. Gayakwaed: OP-amps and Linear Integrated circuits.
[2] K.R. Botkar, Integrated circuits.
[3] Roy Choudhury D, Jain Shail: Linear Integrated circuit", New Age International (P) Limited Publisher, 2008.

References:
[1] Michael Jacob: Applications and Design with Analog Integrated Circuits', PHI, 2nd Edn, 2006
[2] Jacob Milliman and Arvin Grabel: Microelectronics", 2nd Edition, TMH, 2008.

DIGITAL SIGNAL PROCESSING			
Course Code:	**EC206**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: Discrete Time Signals and Systems
Characterization & classification of signals, Typical Signal Processing operations, Discrete-Time Signals, Discrete-Time Systems, Analysis and Implementation of Discrete-Time Linear Time-Invariant Systems, Discrete Time systems described by Difference Equation, Signal flow Graph representation of digital network.

Unit II: The Z-Transform
The Direct z-transform, Properties of the z-transform,ROC, Rational z-transforms, Inversion of the z-transform, analysis of Linear Time-Invariant systems in the z- domain.

Unit III: Finite Fourier Transform
Introduction to DFT - Efficient computation of DFT Properties of DFT - FFT algorithms - Radix-2 FFT algorithms - Decimation in Time - Decimation in Frequency algorithms -Use of FFT algorithms in Linear Filtering and correlation.

Unit IV: Digital Filters Design
Amplitude and phase responses of FIR filters - Linear phase filters - Windowing techniques for design of Linear phase FIR filters - Rectangular, Hamming, Kaiser windows - frequency sampling techniques - IIR Filters - Magnitude response - Phase response - group delay - Design of Low Pass Butterworth filters (low pass) - Bilinear transformation - prewarping, impulse invariant transformation.

Unit V: Finite Word Length Effects
Quantization noise - derivation for quantization noise power - Fixed point and binary floating point number representation - comparison - over flow error - truncation error - co-efficient quantization error - limit cycle oscillation - signal scaling - analytical model of sample and hold operations.

Text Books:
[1] John G Proakis, Dimtris G Manolakis: Digital Signal Processing Principles, Algorithms and Application, PHI, 3rd Edition, 2000.
[2] Johny R.Johnson : Introduction to Digital Signal Processing, Prentice Hall, 1984.

References:
[1] Alan V Oppenheim, Ronald W Schafer, John R Back: Discrete Time Signal Processing, PHI, 2nd Edition 2000.
[2] Avtar singh, S.Srinivasan DSP Implementation using DSP microprocessor with Examples from TMS32C54XX -Thamson / Brooks cole Publishers, 2003.
[3] S.K.Mitra: Digital Signal Processing - A Computer based approach, Tata McGraw-Hill, 1998, New Delhi

ENGINEERING ELECTROMAGNETICS			
Course Code:	**EC208**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: Introduction
Co-ordinate System, Vector Calculus: gradient, divergence, curl, Laplacians of scalar and vector fields. Vector identities.

Unit II: Electrostatics
Coulomb's law – electric field intensity – field due to continuous volume charge, line charge, sheet of charge – stream lines and sketches of fields – electric flux density – gauss's law – application of gauss law – divergence theorem – energy expended in moving a charge in an electric field – potential – potential gradient – dipole – energy density in a electrostatic field. Current and current density – metallic conductors – properties and boundary conditions – method of images – semiconductors – dielectrics – properties and boundary conditions – capacitance – Poisson's and Laplace's equation – uniqueness theorem.

Unit III: Magnetostatics
Biot-Savart law – Ampere's circuital law – curl – Stokes theorem – magnetic flux and flux density – scalar and vector magnetic potentials – steady state magnetic field laws – nature of magnetic materials – magnetization and permeability – boundary conditions –inductance and mutual inductance.

Unit **IV: Time Varying Electromagnetic Fields**
Lorenz Force, Faraday's law – displacement current – Maxwell's equation in point form and integral form – retarded potentials – wave motion in free space, perfect dielectrics, lossy dielectrics – poynting vector and power calculations – propagation in good conductors – reflection of uniform plane waves – standing wave ratio.

Unit V: Transmission Line Theory
Lumped circuit model for transmission line and general solutions. Characteristic impedance, propagation constant, attenuation and phase constants. Open circuited and short circuited lines. Reflection coefficient, transmission coefficient, standing wave pattern, standing wave ratio, return loss and insertion loss. Generator mismatches, distortion in transmission lines. Smith Chart. Impedance matching: single and double stub, quarter wave transformer.

Text book:
[1] William H Hayt: Engineering Electromagnetics, Tata McGraw Hill, New Delhi, 2002.
[2] Surinder P.Seth: Elements of Electromagnetic fields,Dhanpat Rai Publications.

References:
[1] Mathew O Sadiku: Elements of Electromagnetics, Oxford University press, New York, 2003.
[2] David J Griffith: Introduction to Electrodynamics, Pearson Education, 3/e, 2002.
[3] John D Kraus: Electromagnetics, McGraw Hill, New York, 2003
[4] D K Cheng: Field and wave Electromagnetics, Addison Wesley, 2001

DIGITAL SIGNAL PROCESSING LAB			
Course Code:	**EC284**	**Credits:**	**2**
No. of Lectures (Hrs/Week):	**3**	**End Sem Exam Hours:**	**2**
Total No. of Lab sessions:	**10**		**3**

1. Fundamentals of the DSP Processors.
2. Study and Architecture design of DSP chips-TMS 320C 6713 DSP Processor.
3. DSP Programmes in C and Matlab for linear convolution & circular convolution.
4. Matlab Programme for computing discrete convolution and correlation.
5. Matlab Programme for Computing DFT & IDFT.
6. Matlab Programme for Designing the FIR & IIR Filter.
7. Response Analysis of FIR Filter (LP/HP) in Matlab using Windowing technique.
8. Rectangular Window
9. Triangular Window
10. Kaiser Window
11. Response Analysis of IIR Filter (LP/HP) on DSP Processor.
12. Matlab Programme on Fast Fourier Transform applications.
13. Matlab Programme on Power Spectral Density of a Sum of Sinusoidal Signals.

DIGITAL LOGIC DESIGN			
Course Code:	**EC301**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: Introduction
Variables and functions, inversion, truth table, logic gates and networks, Boolean algebra, synthesis using basic gates ,SOP and POS ,NAND and NOR logic networks. Introduction to the CAD tools: Design entry, synthesis, functional simulation, physical design, timing simulation and chip configuration.

Unit II: Logic circuits
Transistor switches, NMOS and CMOS logic gates, Negative logic system,. Fabrication, behavior and on resistance of MOSFET, voltage levels , noise margin, power dissipation, Fan-in, Fan-out and dynamic operation of logic gates.

Unit III: **VHDL**
Digital system design process , Hardware simulation , Levels of abstraction , VHDL requirements ,Elements of VHDL Top down design, VHDL operators, Timing, Concurrency, Objects and classes , Signal assignments ,Concurrent and sequential assignments.

Unit IV: Modeling Techniques
Entity Declaration, Architecture Body, Process statement, Loop control statements, Multiple Processes, Delay Models, Signal Drivers, Block statements, Component declaration and Instantiation, Concurrent Assignment statements, Generics and Configuration, Subprogram, Overloading, Packages and Libraries, Design Libraries,

Unit V: Advance Topics
Introduction to FPGA, CPLD and ASIC Design, Programmable logic devices: PLA and PAL, Hardware Modeling Examples: Modeling of digital modulator and demodulators, digital filters,

Text Book:
[1] J. Bhasker**:** A VHDL Primer, 3rd Edition, PHI.
[2] Brown and Vranesic :Fundamentals of Digital Logic Design, TMH Publication.

References Books:
[1] P.K. Chan & S. Mourad: Digital Design sing Field Programmable Gate Array, PHI.
[2] J. V. Old Field & R.C. Dorf: Field Programmable Gate Array, John Wiley, 1995.
[3] M. Bolton: Digital System Design with Programmable Logic, Addison Wesley, 1990.
[4] Sudhakar Yalamanchili: Introductory VHDL- From Simulation to Synthesis", 3rd Indian Reprint. Pearson Education,
[5] Douglas Perry: VHDL, 3rd Edition, McGraw Hill 2001.

DIGITAL COMMUNICATION SYSTEMS			
Course Code:	**EC303**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: Sampling of Signal, Sampling Theorem for Low Pass and Band Pass Signals, Aliasing, Pulse Amplitude Modulation, Time Division Multiplexing, Channel Bandwidth for PAM-TDM Signal, Types of Sampling, Instantaneous, Natural and Flat Top-Mathematical and Spectral Analysis, Aperture Effect, Introduction to Pulse Position and Pulse Duration Modulation.

Unit II: Pulse Code Modulation: Quantization, Quantization Error, Pulse Code Modulation, Signal-to-Noise Ratio in PCM, Companding, Data Rate and Bandwidth of Multiplexed PCM Signal, Inter-symbol Interference, Eye Diagram, Line Coding ,Differential PCM, Delta Modulation, Adaptive Delta Modulation Slope Overload Error ,Granular Noise ,Comparison of various system in terms of Bandwidth and Signal-to-Noise Ratio.

Unit III: Digital Modulation Techniques:- Analysis, Generation and Detection , Spectrum and Bandwidth of Amplitude Shift Keying, Binary Phase Shift Keying, Differential Phase Shift Keying , Quadrature Phase Shift Keying, M-ary PSK, Binary Frequency Shift Keying, M-ary FSK, Minimum Shift Keying, Quadrature Amplitude Modulation,

Unit IV: Probability of error, bit error rate, Comparison of digital modulation techniques on the basis of probability of error, Matched Filter.

Unit V: Line Coding: Unipolar RZ and NRZ, Bipolar RZ and NRZ, AMI, Split Phase etc. Properties for the selection of Line Codes, HDB Signaling , B8ZS Signaling, Inter-symbol Interference, Nyquist Criteria for Zero ISI, Differential Coding, Regenerative Repeaters, Eye Diagram.

Text Books:

[1] B. Sklar: Digital Communication, Pearson Education
[2] Haykin Simon: Digital Communication, Wiley Publication.

References:

[1] Taub & Schilling: Principles of Communication system, TMH.
[2] Lathi B.P.: Modern Analog and Digital Communication systems, Oxford Uni. Press.
[3] Proakis: Digital communication, McGraw Hill
[4] Schaum's Outline series: Analog and Digital Communication.
[5] Tomasi: Advanced Electronics Communication Systems, 6th Edition, PHI
[6] Singh and Sapre: Communication System, TMH
[7] Couch: Digital and Analog Communication, Pearson Education

ANTENNA AND WAVE PROPAGATION			
Course Code:	**EC305**	**Credits:**	**4**
No. of Lectures (Hrs/Week):	**3+1T**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: Radiation Mechanism
Retarded magnetic potential. Radiated Fields from a Hertzian dipole,halfwave dipole and quarter wave monopole. Power radiated and radiation resistance.

Unit II: Antenna Fundamentals
Radiation intensity, gain, directivity, Power gain, beam width, band width, Reciprocity principle, Effective length and Effective area, Relation between gain effective length and radiation resistance, antenna temperature. FCC Antenna standards A and B. Measurements - radiation pattern- Gain- Directivity and Impedance measurements.

Unit III: Design of Arrays
Linear Array - Two element array, N-element linear array- broadside array, End fire array- Directivity, radiation pattern. Planar array – array factor, beam width, directivity, Circular array-array factor

Unit IV: Design of Antennas

Long wire, V-Antenna, Rhombic antenna, folded dipole antenna, helical antenna, Spiral antenna, Log periodic antenna, Yagi-Uda antenna, Aperture antennas - Horn antenna, parabolic reflector antenna. Microstrip antenna

Unit V: Propagation
Propagation Mechanism- Reflection, refraction and Transmission, Scattering and diffraction. Propagation Model- Path Loss, Free space loss, Plane earth Loss. Noise Modeling, Modes of propagation- Ground wave Propagation, Sky wave Propagation, Space wave, Tropospheric Refraction, Obstruction Loss, Diffraction, Influence of Cluster, Tropospheric effects, Ionospheric Effects, Link budget. Terrestrial fixed Link- Satellite Fixed Link.

Text Books:

[1] E.C.Jordan and Balman: Electro Magnetic Waves and Radiating Systems, PHI, 1968, Reprint 2003.
[2] John D.Kraus and Ronalatory Marhefka: Antennas for all application, Tata McGraw-Hill Book Company, 2002.

References:

[1] R.E.Collins: Antennas and Radio Propagation , McGraw-Hill, 1987.
[2] C A Ballanis : Antenna Theory , John Wiley & Sons, second edition , 2003.

COMPUTER ORGANIZATION AND ARCHITECTURE			
Course Code:	**CS309/CS438**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: Computer Arithmetic and Number System

Number representation; Number System, fixed and floating point number representation, Arithmetic Algorithms (addition, subtraction, Booth Multiplication).

Unit II: **Register Transfer and Micro operation**

Register Transfer Language, Bus and Memory Transfers, Bus Architecture, Bus Arbitration, Arithmetic Logic, Shift Micro operation, Arithmetic Logic Shift Unit, Design of Fast address

Unit III: Processor Design

Processor Organization: General register organization, Stack organization, Addressing mode, Instruction format, Data transfer & manipulations, Program Control, Reduced Instruction Set Computer.

Unit IV: Input-Output Organization

I/O Interface, Synchronous and Asynchronous Data Transfer, strobe, handshaking scheems Modes of transfer, Interrupts & Interrupt handling, Direct Memory access, Input-Output processor.

Unit V: Memory Organization

Memory Hierarchy, Main Memory (RAM and ROM Chips), organization of 2D and $2^{1/2}$ D, Auxiliary memory, Cache memory, Virtual Memory, Memory management hardware.

Text Books:

[1] Patterson, Computer Organisation and Design, Elsevier Pub. 2009.
[2] William Stalling, " Computer Organization", PHI

References:

[1] Vravice,Hamacher & Zaky, "Computer Organization", TMH
[2] Mano," Computer System Architecture", PHI
[3] John P Hays, " Computer Organization", McGraw Hill
[4] Tannenbaum," Structured Computer Organization', PHI
[5] P Pal chaudhry, ' Computer Organization & Design', PHI

DIGITAL COMMUNICATION LAB			
Course Code:	**EC383**	**Credits:**	**2**
No. of Lab (Hrs/Week):	**3**	**End Sem Exam Hours:**	**3**
Total No. of Lab Sessions:	**10**		

List of Experiments

1. To verify the sampling theorem.
2. To study ASK (Amplitude Shift Keying) System.
   - Modulate a digital signal using amplitude shift keying.
   - Demodulate a amplitude shift keyed signal.

3. To study FSK (Frequency Shift Keying) System.
   - Modulate a digital signal using frequency shift keying.
   - Demodulate a frequency shift keyed signal.

4. To study BFSK (Binary Frequency Shift Keying) System.
   - Modulate a digital signal using Binary Frequency shift keying.
   - Demodulate a Binary Frequency Shift keyed signal.

5. To study PSK (Phase Shift Keying) System.
   - Modulate a digital signal using phase shift keying.
   - Demodulate a phase shift keyed signal.

6. To study BPSK (Binary Phase Shift Keying) System.
   - Modulate a digital signal using binary phase shift keying.
   - Demodulate a binary phase shift keyed signal.

7. To study QPSK (Quadrature Phase Shift Keying) System.
   - Modulate a digital signal using Quadrature phase shift keying.
   - Demodulate a Quadrature phase shift keyed signal.

8. To study DPSK (Differential Phase Shift Keying) System.
   - Modulate a digital signal using differential phase shift keying.
   - Demodulate a differential phase shift keyed signal.

9. To study Pulse Code Modulation System (PCM) System.
   - Generate, modulate and transmit a pulse coded signal.
   - Receive and demodulate a pulse coded signal.

10. To study TDM (Time Division Multiplexing) System.
    - Generate and transmit a TDM signal.
    - Receive and de-multiplex a TDM signal.

11. To study M-ARY FSK modulation and demodulation.
12. To study and implement the cyclic redundancy check.
13. To study the circuit of PAM modulator and demodulator.
14. To study the circuit of PWM modulator and demodulator.
15. To study the circuit of PPM modulator and demodulator.

MICROWAVE ENGINEERING			
Course Code:	**EC302**	**Credits:**	**4**
No. of Lectures (Hrs/Week):	**3+1T**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: Introduction
Microwave Frequencies, Microwave Devices, Microwave Systems, Common types of transmission lines- Coaxial, parallel wire, twisted pair, strip line and microstrip lines

Unit II: Waveguides and waveguide components

General solutions for TEM, TE and TM waves- parallel plate waveguide. Rectangular waveguide: TE, TM modes, power transmission, losses in rectangular waveguide, Circular waveguide: TE, TM modes, power transmission, Dielectric fiber and rod waveguide, waveguide coupling, attenuation factor and Q of waveguide. Microwave Hybrid Circuits, Waveguide Tees, Magic Tees (Hybrid Tees), Hybrid Rings (Rat-Race Circuits), Waveguide Corners, Bends and Twists, Directional Coupler, Scattering parameters and Scattering Matrix

Unit III: Microwave Solid State Devices
Introduction, Gunn diode, Ridely-Watkins-Hilsun Theory, Differential Negative Resistance, Modes of Operation, LSA Diodes, InP Diodes, CdTe Diodes, Microwave Generation and Amplification, AVALANCHE TRANSIT-TIME DEVICES, Read Diode, Physical Description, Avalanche Multiplication, Output Power and Quality Factor, IMPATT , TRAPATT BARITT Diodes, Parametric Devices: Nonlinear Reactance and Manley - Rowe Power Relations, Parametric Amplifiers, Applications.

Unit IV: Microwave Tubes
Klystrons, Reentrant Cavities, Velocity-Modulation, Bunching Process, Output Power and Beam Loading, Multicavity Klystron Amplifiers, Beam-Current Density, Output Current Output Power of Two-Cavity Klystron, Output Power of Four-Cavity Klystron, Reflex Klystrons, Velocity Modulation, Power Output and Efficiency, Electronic Admittance, Helix Traveling-Wave Tubes, Slow-Wave structures, Amplification Process, Convection Current, Axial Electric Field, Wave Modes, Gain Consideration, MICROWAVE CROSSED-FIELD TUBES, Magnetron Oscillators, Cylindrical Magnetron, Coaxial Magnetron, Ricke diagram.

Unit V: Microwave Measurements
Measurement of unknown impedance using Slotted line, VSWR measurement, attenuation measurements- measurement of scattering parameters , measurement of dielectric constant.

Text Books:
[1] Samuel Y. Liao: Microwave Devices and Circuits - Prentice Hall of India - 3rd Edition (2003).
[2] David M. Pozar: Microwave Engineering. - John Wiley & Sons - 2nd Edition (2003).

References:
[1]R.E. Collin: Foundations for Microwave Engineering - IEEE Press Second Edition (2002).
[2]Annapurna Das and Sisir K.Das: Microwave Engineering - Tata McGraw-Hill (2000)

MICROPROCESSORS AND INTERFACING			
Course Code:	**EC304/EC559**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: Introduction to 8085 microprocessor: Pin diagram, architecture, programming model, instruction set, and classification of instruction set, instruction and data format, timing diagram of instructions. Basic concept of programming, Addressing Modes of 8085 microprocessors

Unit II: Microprocessor 8086 Architecture - BIU and EU, Registers, Pin Diagram, Memory Addressing, Clock Generator 8284, Buffers and Latches, Maximum and Minimum Modes

Unit III: Addressing Modes, Instruction set of 8086, Assembly Language Programming, Assemblers, Procedures, Macros, Interrupts, 8086 Based Multiprocessor Systems

Unit IV: Interfacing Chips- IC 8155 (Static Ram with I/O Ports and Timer), 8755 (EPROM with I/O Ports), 8251A (USART), 8255A(Programmable Peripheral Interface), 8253/8254 (Programmable Interval Timer/Counter), 8257 (DMA Controller), 8259A (Programmable Interrupt Controller)

Unit V: The 8051 architecture Microprocessor and Microcontroller, Comparison of microprocessors and microcontrollers Microcontroller survey – microcontrollers of different word length, make and features, selection criteria for microcontroller ,8051 microcontroller hardware – I/O pins and internal architecture internal RAM,ROM organization , I/O port circuits ,connecting external memory, addressing modes , Instruction set and assembly language programming.

Text Books:
[1] A K Ray : Advanced Microprocessors and Interfacing, 2nd edition,TMH
[2] Mazidi and Mazidi: The 8051 Microcontroller and Embedded Systems, Pearson Education

References:
[1] B. B. Brey: The Intel Microprocessors, Architecture, Programming and Interfacing, Pearson Education.
[2] Liu Gibson: Microcomputer Systems: The 8086/8088 Family- Architecture, Programming and Design, PHI
[3] D. V. Hall: Microprocessors and Interfacing, TMH.
[4] Ayala Kenneth:The 8051 microcontroller, Third Edition, Cengage Learning
[5] A. V. Deshmukh: Microcontroller (Theory and Application), TMH.
[6] Raj Kamal: Embedded Systems- Architecture, Programming and Design, TMH, New Delhi.
[7] V. Udayashankara and M. S. Mallikarjunaswamy: 8051 Microcontroller, TMH, New Delhi.
[8] R S Gaonkar, Microprocessor, Architecture, Programming, and Applications with the 8085, Penram International Publication, 5/e
[9] P.K. Ghosh and P. R. Sridhar, 0000 to 8085 Introduction to microprocessor for Engineers and Scientists, PHI, 2/e

MICROELECTRONICS ENGINEERING			
Course Code:	**EC306/EC446**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: MOSFETS

Device Structure and Physical Operation, V-I Characteristics, MOSFET Circuits at DC, Biasing in MOS amplifier Circuits, Small Signal Operation and Models, MOSFET as an amplifier and as a switch, biasing in MOS amplifier circuits, small signal operation. MOSFET internal capacitances and high frequency mode, CMOS digital logic inverter, detection type MOSFET.

Unit II: Single Stage IC Amplifier

IC Design philosophy, comparison of MOSFET and BJT, Current sources, Current mirrors and Current steering circuits, high frequency response, CS and CF amplifiers, CG and CB amplifiers, Cascade amplifiers, CS and CE amplifiers with source (emitter) degeneration source and emitter followers, some useful transfer parings, current mirrors with improved performance.

Unit III: Differential and Multistage Amplifiers

MOS differential pair, small signal operation of MOS differential pair, the BJT differences pair, other non-ideal characteristics and differential pair, Differential amplifier with active loads, frequency response and differential amplifiers, Multistage amplifier.

Unit IV: Feedback and Operational Amplifiers

General Feedback structure, properties of negative feedback, basic feedback topologies, loop gain, Stability problem, effect of feedback on amplifier poles, stability analysis by Bode plots, frequency compensation. Two stage CMOS Op-amp, folded cascade CMOS op-amp, 741 op-amps. Data Converters, A-D and D-A converters.

Unit V: Digital CMOS circuits

Overview. Design and performance analysis of CMOS inverter. Logic Gate Circuits. Pass-transistor logic. Dynamic Logic Circuits.

Text Books:

[1] Adel Sedra and K.C. Smith, Microelectronic Circuits, 5th Edition, Oxford Uni. Press, 2004.
[2] Richard C. Jaeger and Blalock, Microelectronic Circuit Design,3rd Edition, TMH 2007

References:

[1] Behzad Razavi, Fundamentals of Microelectronics, John Wiley, 2008

INFORMATION THEORY AND CODING			
Course Code:	**EC308**	**Credits:**	**4**
No. of Lectures (Hrs/Week):	**3+1T**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: Probability, random variables, probability distribution and density functions, joint statistics, conditional statistics, independence, function of random variables and random vectors, expectation, moments, characteristic functions, convergence of a sequence, Central Limit theorem, random processes, , mean, autocorrelation, stationary ergodicity, power spectral density, Gaussian, Poison, and Markovian processes

Unit II: Information, Amount of Information, Unit of Information, Average Information or Entropy, Information Rate, Joint and Conditional Entropy, Discrete Memoryless Channel-Channel representation, channel matrix, properties of channel matrix, Special channels-(Lossless, Deterministic, Noiseless, Binary Symmetric Channel, Binary Channel, Binary Erasure Channel

Unit III: Mutual Information and Channel Capacity, Mutual Information and Channel Capacity for Special Channels. Coding to increase Average Information per Bit, Shannon's Theorem & Its Application, Capacity of Gaussian Channel, Shannon Hartley Theorem, Bandwidth & S/N Trade off

Unit IV: Source coding, Code Length and Code Efficiency , Source Coding Theorem, Fixed Length Codes, Variable Length Codes, Distinct Code, Prefix-free Codes, Uniquely Decodable Codes, Instantaneous Codes, Optimal Codes, Kraft Inequality.

Unit V: Source Coding Techniques: Shannon Fano and Huffman Coding Algorithms. Coding Efficiency Error control coding : Linear Block Codes, Systematic Linear Blocks Codes, Parity Check Matrix, Syndrome Testing, Cyclic code, Hamming Code, Error Detection and Correction Codes, Convolution Codes: State Diagram, Tree Diagram and Trellis Diagram, Maximum Likelihood Decoding, Viterbi decoding.

Text Books:
[1] Taub & Schilling, Principles of Communication system, TMH.
[2] Lathi B.P., Modern Analog and Digital Communication systems, Oxford Uni. Press.

References:
[1] Haykin Simon, Digital Communication, Wiley Publication.
[2] Proakis, Digital communication, McGraw Hill
[3] Schaum's Outline series, Analog and Digital Communication.
[4] B. Sklar, Digital Communication, Pearson Education.
[5] Tomasi: Advanced Electronics Communication Systems, 6th Edition, PHI
[6] Singh and Sapre: Communication System, TMH
[7] Couch: Digital and Analog Communication, Pearson Education

PRINCIPLES OF COMPUTER NETWORKS			
Course Code:	**CS310**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I INTRODUCTION OF NETWORK MODEL

Principal of computer Network, Internet, protocols and standards, network models, layered task, internet model, peer-peer processes, functions of layers, OSI model and TCP/IP model.

UNIT II Physical Layer

Analog and digital, analog signals, digital signals, analog vs. digital, data rate limit, transmission, digital transmission, line coding, block coding, sampling, transmission mode, modulation and digital data, telephone modem, modulation of analog signals, multiplexing: FDM, WDM, TDM. Guided media, unguided media, radio waves, microwaves, infrared, circuit switching, and telephone network.

UNIT III DATA LINK LAYER

Space division switch, time division switch, TDM bus, telephone network, high-speed digital access: DSL, cable modems and SONET, DSL technology, types of errors, detection, error correction. Flow and error control, ARQ, HDLC, point-to-point access, PPP stack, multiple access, ALOHA, random access, controlled access, channelization, LAN, Ethernet, wireless LANs, IEEE 802.11, bluetooth, connecting device, cellular telephone and satellite network circuit switching, frame relay.

UNIT IV NETWORK LAYER AND TRANSPORT LAYER

Routing and routing algorithms, addressing, IPv4, ICMP, ARP, IPv6 and ICMPv6 extensions and functionality, mobile IP, service integration and quality of service (QoS) in IP networks. Transport services, element of transport protocols, TCP and UDP, RTP, SCTP, congestion control and congestion avoidance, integrated services.

Unit V: Application Layer

Introduction to Application layer, SMTP, HTTP, Remote login, DNS, FTP, DHCP.

Reference Books:

1. Data Communications and Networking, Forouzan, 4th edition, McGraw Hill, 2007.
2. Data and Computer Communications, W. Stallings, 8th edition, Prentice Hall, 2007.
3. Computer Networks, S. Tanenbaum, 4th edition, Prentice Hall, 2003.
4. Internetworking With TCP/IP Volume 1: Principles Protocols, and Architecture, Douglas E Comer, 5th edition, PHI.
5. TCP/IP Protocol Suite, B.A. Forouzan, TMH, 3rd edition, 2006.

COMPUTER NETWORKS			
Course Code:	**CS308**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: Introduction and Physical Layer
Key concepts of computer network, Transmission media, Network devices, Network topology, Topology design issues, Types of network: LAN, MAN, WAN, PAN, ISDN systems and ATM network, OSI-reference model, open system standards, Characteristics of network, TCP/IP model, Protocols and standards, Encoding Technique.

Unit II: Switching and Data Link Layer
Circuit switching, Packet switching, Message switching, Hybrid switching, and ATM switching. Multiplexing Techniques: TDMA, FDMA, WDMA, CDMA, Data link layer: LLC & MAC level protocols and design issues, issues IEEE 802 LAN Standards, framing, CRC, Error control, Flow control, HDLC, ALOHA and performance issues. Frames relay networks and performance parameters.

Unit III: Network Layer
Network layer design issues, overview of IPv4 and IPv6, Addressing: class full and classless, static and dynamic, subnet and supernet, Autoconfiguration through DHCP, Routing Protocols: RIP, DVR,LSR, OSFP, BGP, Congestion control algorithm, Subnet concept, Virtual LAN, ICMP, Multicasting, Mobile IP.

Unit IV: Transport Layer
Port addressing schemes, connectionless and connection oriented services: TCP and UDP, wireless TCP, Congestion control, Queue Management, NAT, PAT, Socket Format at transport level, socket interface and programming.

Unit V: Application Layer
Client Server Architecture, Domain Name Services, Application services: HTTP, TELNET, RLOGIN, FTP, CBR, NFS, SMTP, POP, IMAP, MIME, Voice and video over IP

Text Books:
[1] S. Tanenbaum, Computer Networks, 4th edition, Prentice Hall, 2008
[2] Data and Computer Communications, W. Stallings, 8th edition, Prentice Hall, 2007

References:
[1] TCP/IP Principles, Protocols and Architecture, Douglus E. Comer, Pearson Education
[2] F. Haball ,Data Communication, Computer network & open systems - Computer Networks : An Engineering approach - S. Keshav

MICROPROCESSOR AND INTERFACING LAB			
Course Code:	**EC384/EC587**	**Credits:**	**2**
No. of Lectures (Hrs/Week):	**3**	**End Sem Exam Hours:**	**3**
Total No. of Lab Sessions:	**10**		

List of Experiments:

1. Addition of two 8-bit numbers, result 8-bit.
2. Addition of two 8-bit numbers, result 16-bit.
3. Subtraction of two 8-bit numbers.
4. Addition of two 16-bit numbers.
5. Multiplication of two 8-bit numbers.
6. Division of two 8-bit numbers.
7. 2's Compliment of a 8-bit number.
8. Arrange the array in ascending order.
9. Arrange the array in descending order.
10. Moving the block of data from one memory location to another memory location.
11. Largest number in an array.
12. Smallest number in an array.
13. BCD to HEX conversion.
14. HEX to BCD conversion.
15. HEX to ASCII conversion.
16. ASCII to HEX conversion.
17. Square of a number using lookup table method.
18. Interfacing of 8255.
19. Interfacing of 8253/8354.

1. Interfacing of 8237/8257.

2. Interfacing of 8259.

3. Interfacing of 8251.

OPTICAL COMMUNICATION			
Course Code:	**EC401**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: Introduction

Forms of communication system, evolution of fiber optic system, elements of a fiber transmission link, advantages of optical fiber communication

UNIT II: Optical Fibers

The nature of light, basic optical Laws, fiber types, electromagnetic theory of propagation of light in optical fibers, waveguide equations for step index fibers, modes in step index fiber, power flow in the step index fibers, graded index fiber, modes in graded index fiber. Fiber fabrication: outside vapor phase oxidation, vapor phase axial deposition, modified chemical vapor deposition, double crucible method, and mechanical properties of fibers. Signal degradation in optical fibers: absorption, scattering losses, bending loss, material dispersion, waveguide dispersion, intermodal distortion, pulse broadening in graded index waveguides. Fiber to fiber joints, fiber end face preparation. Fiber splicing: splicing techniques, optical fiber connectors.

Unit III: Optical Sources

Types of optical sources, Lasers: basic concepts, absorption and emission of radiation, population inversion, optical feedback and laser oscillation, p-n junction, spontaneous emission, stimulated emission and lasing, laser modes, single mode operation, non-semiconductor laser, Light emitting diodes: the double heterojunction LED, Planner LED, surface emitter LEDs, edge emitter LEDs, LED characteristics, optical output power, output spectrum, modulation bandwidth, reliability.

Unit IV: Detectors and Amplifiers

Device type, optical detection principles, absorption, quantum efficiency, responsivity, long wavelength cutoff, semiconductor photodiodes without internal gain, photodiodes with internal gain, phototransistors, photoconductive detectors, Optical amplifiers: semiconductor amplifiers, fiber amplifiers

Unit V: Advanced Systems And Applications

Wavelength Division Multiplexing, local area networks, photonic switching, nonlinear optical effects. Public network applications: trunk network, junction network, local access network, synchronous networks, military applications, optical sensor systems, computer applications

Text Books:

[1] Senior, J M, "Optical Communication Principle and Practices", II edition Pearson Education Ltd, 2006.
[2] Keiser G, "Optical Fiber communications", second edition, McGrawhill. Inc.1993.

REFERENCES:

[1] Biswas Sambhu Nath, 'Optoelectronic Engineering", Dhanpat Rai Publication1994.
[2] Gowar J., optical communication systems, PHI.
[3] William B. Jones jr., Introduction to optical fiber communication systems, Holt,Rinehart and Winston, Inc

SEMICONDUCTOR DEVICE MODELLING AND TECHNOLOGY			
Course Code:	**EC403**	**Credits:**	**4**
No. of Lectures (Hrs/Week):	**3+1T**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: Introduction
Semiconductors, Conduction Mechanism, Contact Potentials, PN Junctions, Flat Band voltages, Potential Balance and Charge Balance, Depletion and Inversion Regions, Small Signal Capacitance.

Unit II: MOS Transistor Models
Contacting the inversion layer, Body Effect, Pinch Off Voltage, General Charge Sheet Model, Models based on Quasi Fermi potentials, Region of Inversions in terms of terminal volatages, Source Referenced and body referenced modeling, Effective mobility, Temperature effects, Breakdown.

Unit III: MOS Transistor with Ion Implanted Models
Charges and Threshold voltages, Drain to Source Current Model for strong inversion, Depletion MOSFets, need for n type implant, Surface Channel Enhancement Mode NMOS and PMOS, channel length Modulation, Punch Through, Barrier Lowering.

Unit IV: MOS Transistor Large Signal Modeling
Quasi Static operation, Quasi Static Models and its limitations, Non Quasi Static Modeling, The continuity equation, Non Quasi Static Analysis.

Unit V: MOS Small Signal Models
Law Frequency small signal model: Strong, Weak and Moderate Inversions, Medium Frequency small Signal Models, Intrinsic capacitances, White noise, Flicker Noise, Small Dimensions effects, High Frequency small signal models, High Frequency noise.

Text Books:
[1] Operation and Modelling of the MOS Transistor, Yannis Tsividis.

References:
[1] Carlos Galup Montoro: CMOS Analog Design using All Region MOSFET Modeling, Cambridge University Press.
[2] Guide Yuhua Cheng, Chenming Hu: MOSEFET Modeling and BSIM3 User's.

WIRELESS MOBILE COMMUNICATION			
Course Code:	**EC405**	**Credits:**	**4**
No. of Lectures (Hrs/Week):	**3+1T**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: Cellular concept, frequency reuse, channel assignment schemes, handoff strategies, interference and system capacity, trunking, grade of service, coverage and capacity enhancement techniques

Unit II: Mobile radio propagation-free space propagation model, two ray model, link budget using path loss models, outdoor and indoor propagation models, small scale fading-multipath propagation, IR model, multipath measurements, parameters of multipath channels, small scale fading, statistical models for multipath fading channels

Unit III: Modulation techniques-overview of digital modulation, line coding, pulse shaping techniques, spread spectrum modulation-PN sequence, DS-SS, FH-SS, modulation performance in fading and multipath channels, speech coding-vocoder, LPC

Unit IV: Multiple access techniques-FDMA, TDMA, spread spectrum multiple access- FHMA, CDMA, SDMA, packet radio-protocols, CSMA protocols, reservation protocols, capacity of cellular systems

Unit V: GSM-services and features, architecture, radio sub systems, channels types, frame structure and signal processing, CDMA-specifications, forward and reverse CDMA channels, CT2, DECT, PACS, PDC, PHS

Text books:

[1] Theodore S. Rappaport, " Wireless Communication, Principles and Practice" Pearson
[2] Kaveh Pahlavan, Prashant Krishnamurthy, " Principles of Wireless Networks", PHI

References:

[1] W.C. Jakes: Microwave Mobile Communication, IEEE Press
[2] Kaveh Pahlavan & Allen H. Levesque: Wireless Information Networks, Wiley series in Telecommunications and signal processing.
[3] Kamilo Feher: Wireless Digital communications, Modulation and Spread Spectrum Applications. PHI

DESIGN WITH MICROCONTROLLERS			
Course Code:	**EC441**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: The 8051 architecture
Microprocessor and Microcontroller, Comparison of microprocessors and microcontrollers Microcontroller survey –microcontrollers of different word length, make and features, selection criteria for microcontroller, 8051microcontroller hardware – I/O pins and internal architecture internal RAM, ROM organization, I/O port circuits, connecting external memory

Unit II: Assembly Language Programming
Addressing modes, data transfer, arithmetic, logical, branch transfer, stack and bit related instructions Programming 8051for basic operations, connecting 8255 ,Programming tools and techniques

Unit III: Interrupts
Timer interrupt, serial port interrupt, external interrupt, reset, interrupt control, interrupt priority Interrupt destinations ,software generated interrupts, connecting A/D and D/A ,application programs using interrupt.

Unit IV: Counter and timers
Timer modes of operation ,timer counter interrupt ,counter ,serial data transmission ,reception, Serial data transmission modes , programming based on timer application and serial transmission.

Unit V: Interfacing and applications
Scanning programs for small keyboards interrupt driven programs, program for matrix keyboard LCD display, frequency measurement, pulse measurement, multiple interrupts, measurement and control of physical parameter as Temperature, stepper motor control

Text Books:
[1] Mazidi Mazidi McKinley, the 8051 Microcontroller & Embedded system Using Assembly and C, 2/E Pearson Education, 2006
[2] Kenneth J.Ayala, The 8051 Microcontroller, 3/E Penram International, 2007.

Reference Books:
[1] A. V. Deshmukh: Microcontroller (Theory and Application), TMH.
[2] Raj Kamal: Embedded Systems- Architecture, Programming and Design, TMH, New Delhi.
[3] V. Udayashankara and M. S. Mallikarjunaswamy: 8051 Microcontroller, TMH, New Delhi.

TELECOMMUNICATION SWITCHING AND NETWORKS			
Course Code:	**EC443**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit-I: Digital switching systems-analysis, hierarchy, evolution, SPC, call processing, communication and control- level 1,2,& 3 control, interface control, network control processor, central processor, control architecture, multiplexed highways, switching fabric-space division switching, time division switching, STS, TST, TTT, switching system software-architecture, OS, database management

Unit-II: MPLS-label stack and label distribution, traffic engineering, design of switching systems, and routers, switching networks-crossbar switches, multistage switches, shared memory switches, optical networks, and WDM techniques, , IP over optical core switches

Unit-III: Congestion control: integrated services, differentiated services, congestion control, congestion control in packet switching, frame relay congestion control, flow control at link level, TCP congestion control

Unit-IV: Voice over IP: basic IP telephone system, digital voice sampling, compression techniques, protocol for VoIP, session initiation protocol,

Unit-V: Frame relay, ATM, protocol architecture, logical connections, cells, AAL, High speed LAN, Ethernet, Fiber channel

Text books:

[1] Syed R. Ali, "Digital Switching Systems, System Reliability and analysis, Tata McGraw-Hill
[2] William Stallings, "High Speed Networks and Internet" 2nd ed. Pearson Ed., 2005

Reference:

SATELLITE COMMUNICATION			
Course Code:	**EC445**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit-I

Overview of satellite systems: Introduction, Frequency allocations for satellite systems.

Orbits and launching methods: Kepler's three laws of planetary motion, terms used for earth orbiting satellites, orbital elements, apogee and perigee heights, orbit perturbations, inclined orbits, local mean solar point and sun-synchronous orbits, standard time.

Unit-II

The Geostationary orbit: Introduction, antenna look angles, polar mount antenna, limits of visibility, near geostationary orbits, earth eclipse of satellite, sun transit outage, launching orbits.

Polarization: antenna polarization, polarization of satellite signals, cross polarization discrimination.

Depolarization: ionospheric, rain, ice.

Unit-III

The Space segment: introduction, power supply, attitude control, station keeping, thermal control, TT&C subsystem, transponders, antenna subsystem, Morelos and Satmex 5, Anik-satellites, Advanced Tiros-N spacecraft.

The Earth segment: introduction, receive-only home TV systems, master antenna TV system, Community antenna TV system, transmit-receive earth station.

Unit-IV

The space link: Introduction, Equivalent isotropic radiated power (EIPR), transmission losses, the link power budget equation, system noise, carrier-to-noise ratio (C/N), the uplink, the downlink, effects of rain, combined uplink and downlink C/N ratio, inter-modulation noise, inter-satellite links. Interference between satellite circuits.

Unit-V

Satellite services

VSAT (very small aperture terminal) systems: overview, network architecture, access control protocols, basic techniques, VSAT earth station, calculation of link margins for a VSAT star network.

Direct broadcast satellite (DBS) Television and radio: digital DBS TV, BDS TV system design and link budget, error control in digital DBS-TV, installation of DBS-TV antennas, satellite radio broadcasting.

Text Books:

[1] D. Roddy: Satellite Communications, 4th Edition, TMH, New Delhi.
[2] T. Pratt, C. Bostian and J. Allnut: Satellite Communications, 2nd Edition, Wiley India
[3] D.C. Agarwal: Satellite Communications, Khanna Publishers.

References:

[1] W. L. Pritchard, H. G. Suyderhoud and R. A. Nelson: Satellite Communication Systems Engineering, 2nd Edition, Pearson Education.
[2] R. M. Gangliardi: Satellite Communications, CBS Publishers.
[3] M. R. Chartrand: Satellite Communication, Cengage Learning.
[4] Raja Rao: Fundamentals of Satellite communications, PHI Learning.
[5] Monojit Mitra: Satellite Communication: PHI Learning.

DIGITAL IMAGE PROCESSING			
Course Code:	**EC447**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: Digital Image Processing (DIP)
Introduction, examples of fields that use DIP, fundamental Steps in DIP, components of an image processing System., Digital Image Fundamentals- elements of visual perception, image sensing and acquisition, image sampling and quantization, basic relationships between pixels

Unit II: Image Transforms
Two-dimensional (2-D) impulse and its shifting properties, 2-D continuous Fourier Transform pair, 2-D sampling and sampling theorem,2-D Discrete Fourier Transform (DFT), properties of 2-D DFT.Other transforms and their properties: Cosine transform, Sine transform, Walsh transform, Hadamard transform, Haar transform, Slant transform, KL transform.

Unit III: Image Enhancement
Spatial domain methods-basic intensity transformation functions, fundamentals of spatial filtering, smoothing spatial filters (linear and non-linear), sharpening spatial filters (unsharp masking and highboost filters), combined spatial enhancement method.Frequency domain methods- basics of filtering in frequency domain, image smoothing filters (Butterworth and Guassian low pass filters), image sharpening filters (Butterworth and Guassian high pass filters), selective filtering.

Unit IV: Image Restoration
Image degradation/restoration, noise models, restoration by spatial filtering, noise reduction by frequency domain filtering, linear Position invariant degradations, estimation of degradation function, inverse filtering, Wiener filtering, image reconstruction from Projection.

Unit V: Image Compression
Fundamentals of data compression- basic compression methods: Huffman coding, Golomb coding, LZW coding, Run-Length coding, Symbol based coding. Digital Image Watermarking, Representation and Description- minimum perimeter polygons algorithm (MPP).

Text Books:
[1] R. C. Gonzalez and R. E. Woods: Digital Image Processing, 3rd Edition, Pearson Education.
[2] A. K. Jain: Fundamentals of Digital Image Processing, PHI Learning.
[3] S. Annadurai and R. Shanmugalakshmi: Fundamentals of Digital Image Processing, Pearson Education.

References:
[1] M. Sonka, V. Hlavac and R. Boyle: Digital Image Processing and Computer Vision: Cengage Learning.
[2] B. Chanda and D. D. Majumder: Digital Image Processing and Analysis, PHI Learning.
[3] S. Jayaraman, S. Esakkirajan and T. Veerakumar: Digital Image Processing, TMH.

COMMUNICATION NETWORKS AND TRANSMISSION LINES			
Course Code:	**EC449**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I:
Characteristic Parameters of symmetrical and asymmetrical two port networks and their design: image impedance, iterative impedance, characteristic impedance, propagation coefficient, image transfer coefficient ,iterative transfer coefficient, Lattice and Bridged-T networks, reactive matching networks, matching techniques, Insertion Loss, symmetrical and asymmetrical attenuators and their design.

Unit II:
Passive LC Filters: Analysis and design of Low pass, high pass, band pass and band elimination filters, m-derived filters, composite filters, Filter specifications, Butterworth approximation, Chebyshev approximation, elliptic function approximation, frequency transformation.

Unit III:
Positive real function, LC, RL, RC, and RLC network synthesis, Foster and Cauer network, minimum positive real function, Brune's method, Bott-Duffin method, Synthesis-Coefficient.

Unit IV:
Transmission line fundamentals: Lumped parameter equivalent, voltage and current on a transmission line, infinite line, characteristic impedance and propagation constant, waveform distortion, attenuation and phase equalizers, distortion-less line, loading, liner reflection on a line, reflection coefficient, input and transfer impedances, open circuit and short circuit line, reflection factors, reflection loss, insertion loss, T and π equivalents of a line, location of line fault. Construction and design of two wire line and coaxial cable.

Unit V:
Line at radio frequencies, parameters of line and coaxial cable at radio frequencies, dissipation-less line, voltage and current on a dissipation-less line, standing waves, standing wave ratio, input impedance of open circuit and short circuit, power and impedance measurement on lines, eighth-wave, quarter-wave and half wave line, circle diagram, Smith chart, solution of problems using Smith chart, single and double stub matching .introduction to micro-strip linesand its analysis.

Text Book:
[1] J.D. Ryder: Networks and Transmission Lines, 2nd edition, PHI
[2] Umesh Sinha: Networks and Transmission Lines, Satya Prakashan.

References:
[1] M.E. Valkenberg: Introduction to Modern Network synthesis, Wiley Eastern Ltd.
[2] G.K. Mithal: Network Analysis, Khanna Publishers.
[3] Suresh: Electric Circuits and Networks, Pearson Education.

PRINCIPLES OF VLSI DESIGN			
Course Code:	**EC465/EC555**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: Basic MOS Technology
Integrated circuit's era. Enhancement and depletion mode MOS transistors. nMOS fabrication. CMOS fabrication. Thermal aspects of processing. BiCMOS technology. Production of E-beam masks.MOS Device Design Equations, The Complementary CMOS Inverter: DC Characteristics, Static Load MOS Inverters, The Differential Inverter, The Transmission Gate, Tristate Inverter.

Unit II: Circuit Design Processes and CMOS Logic Structures
MOS layers, Stick diagrams, Design rules and layout – lambda-based design and other rules, Layout diagram, Symbolic diagrams, Basic Physical Design of Simple logic gates, CMOS Complementary Logic, Bi CMOS Logic, Pseudo-nMOS Logic, Dynamic CMOS Logic, Clocked CMOS Logic, Pass Transistor Logic, CMOS Domino Logic Cascaded Voltage Switch Logic.

Unit III: MOS Circuits Concepts
Sheet resistance, Area capacitances, Capacitance calculations, delay unit, Inverter delays, Driving capacitive loads, Propagation delays, Wiring capacitances, Scaling models and factors, Limits on scaling, Limits due to current density and noise.

Unit IV: CMOS Subsystem Design and Processes
Architectural issues, Switch logic, Gate logic, Design examples – combinational logic, Clocked circuits, other system considerations, Clocking Strategies, Subsystem design processes: General considerations, Process illustration, ALU subsystem, Adders. Multipliers.

Unit V: Advance Topic
Memory registers and clock: Timing considerations. Memory elements, Memory cell arrays. Testability: Performance parameters. Layout issues. I/O pads, System delays, Ground rules for design, Test and testability.

Text Books:
[1] CMOS VLSI Design – A Circuits and Systems Perspective, 3rd Edition, N.H. Weste and David Harris. Addison- Wesley, 2005.
[2] Basic VLSI Design - Douglas A. Pucknell & Kamran Eshraghian, PHI 3rd Edition, 2005.

Reference Books:
[1] Principles of CMOS VLSI Design: A Systems Perspective, Neil H. E. Weste, K. Eshragian, Pearson Education (Asia) Pvt. Ltd.

RADAR AND TV ENGINEERING			
Course Code:	**EC467**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: Elements of system of television, scanning sequence, interlacing determination of bandwidth synchronizing pulses, equalizing pulse, composite video signal, television camera tubes, monochrome picture tube.

Unit-II: Television transmitter, block diagram of T.V receiver, video detector design and operation of sound signal, transmitting and receiving antennas.

Unit III: Basic principle of colour T.V, three colour theory, colour mixing, chromaticity chart, colour picture tube, delta gun, PIL and Trinitron picture tube, PAL, SECAM and NTSE ystems, brief introduction of VCP and VCR, introduction of HDTV.

Unit IV: Introduction to radar, radar frequencies, radar block diagram, radar equation and its performance factors such as cross section and its fluctuation, transmitter power, pulse repetition frequency. Antenna parameters, system losses and propagation effect.

Unit V: Doppler effect, CW radar, frequency modulated and multiple Doppler frequency radar, oving target indication radar, delay line canceller blind speed, duplexer, scanning and racking radar, lobe switching, monopoles, conical scan,Adcock antenna, instrument ending system (ILS) ground controlled approach(CGA) kit port surveillance radar (PSR), precision approach radar(PAR).

Text Books:

[1]. R. R. Gulati: Monochrome and Colour Television, New Age Publication.
[2]. M. I. Skolnik: Introduction to Radar Systems, TMH, New Delhi.
[3]. M. Dhake: Television and Video Engineering, 2nd Edition,TMH, New Delhi.

References:

[1]. R. G. Gupta: Television Engineering and Video Systems, TMH, New Delhi.
[2]. Grob and Herndon: Basic Television and Video Systems, McGraw Hill International.
[3]. P. Z. Peebles, Jr.: Radar Principles, Wiley India Pvt. LTD.
[4]. Edde: Radar-Principles, Technology Applications, Pearson Education.

VLSI TECHNOLOGY			
Course Code:	**EC536**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Crystal Growth, Wafer Preparation, Epitaxy and Oxidation
Electronic Grade Silicon, Czochralski crystal growing, Silicon Shaping, processing consideration, Vapor phase Epitaxy, Molecular Beam Epitaxy, Silicon on Insulators, Epitaxial Evaluation, Growth Mechanism and kinetics, Thin Oxides, Oxidation Techniques and Systems, Oxide properties, Redistribution of Dopants at interface, Oxidation of Poly Silicon, Oxidation induced Defects.

UNIT II: Lithography and Relative Plasma Etching
Optical Lithography, Electron Lithography, X-Ray Lithography, Ion Lithography, Plasma properties, Feature Size control and Anisotropic Etch mechanism, relative Plasma Etching techniques and Equipments

UNIT III: Deposition, Diffusion, Ion Implantation and Metallization
Deposition process, Polysilicon, plasma assisted Deposition, Models of Diffusion in Solids, Flick's one dimensional Diffusion Equation – Atomic Diffusion Mechanism –Measurement techniques - Range theory- Implant equipment. Annealing Shallow junction – High energy implantation – Physical vapour deposition – Patterning.

UNIT IV: Process Simulation and VLSI Process Integration
Ion implantation – Diffusion and oxidation – Epitaxy – Lithography – Etching and Deposition- NMOS IC Technology – CMOS IC Technology – MOS Memory IC technology - Bipolar IC Technology – IC Fabrication.

UNIT V: Assembly Techniques and packaging of VLSI Devices
Analytical Beams – Beams Specimen interactions - Chemical methods – Package types – banking design consideration – VLSI assembly technology – Package fabrication technology.

Text Books:
[1] S.M.Sze: VLSI Technology, Mc.Graw Hill Second Edition. 2002.
[2] Richard Jaegar, Introduction to Microelectronics Fabrication, Addison-Wesley, 2006.
[2] Douglas A. Pucknell and Kamran Eshraghian: Basic VLSI Design, Prentice Hall India, 2003.

References:
[1] Amar Mukherjee: Introduction to NMOS and CMOS VLSI System design, Prentice Hall India, 2000.
[2] Wayne Wolf : Modern VLSI Design, Prentice Hall India,1998.
[3] Plummer, Deal and Graffin, Silicon VLSI Technology: Fundamentals, Practice and Modeling, Prentice Hall, 2000

ADVANCED ANALOG VLSI DESIGN			
Course Code:	**EC538**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I- Introduction
Basic building blocks in Analog ICs, Translinear networks, Video and RF/IF Amplifiers, IC negative feedback wide band amplifiers, Voltage Sources and References, IC Voltage Regulator, Characteristics and Parameters of Voltage, Protection circuitry for Voltage Regulator, Switched Mode Regulator, IC Voltage Op Amps, Transconductance Op Amps, Audio Power and Norton's Amplifier, Analog Multipliers, Voltage Controlled Oscillator, Self Tuned Filter, Phase Locked Loop, Current Mode ICs.

UNIT II – CMOS Analog Circuit Design
Submicron, Deep Submicron and Ultra-Deep Submicron CMOS Technology, BiCMOS Technology, Latchup and ESD, MOS Capacitor Model, Large Signal Model Dependence, Small Signal Models, Noise, Passive Component Models, Component Matching, Computer Models and Extraction of the Simple Large Signal Model, MOS Switch, Current Sinks and Sources.

UNIT III – High Speed Operational Amplifiers & Comparators Design
Two-stage Op Amp Design, Simulation and Measurement of Op Amps, Buffered Op Amps, High Speed Op Amps, Differential-In, Differential-Out Op Amps, Low Noise and Low Power Op Amps, Low Voltage Op Amps, Open-Loop Comparators, Improved Open-Loop Comparators and Latches, High speed comparators

UNIT IV – Design of ADCs & DACs
Characterization of DACs and Current Scaling DACs, Voltage, Charge Scaling and Serial DACs, Improved Resolution, Characterization of ADCs and Sample and Hold Circuits, Moderate Speed Nyquist ADCs, High Speed Nyquist ADCs, Oversampling ADCs.

UNIT V – Advance Topics
Analysis and optimized design of integrated analog systems and building blocks, Specific topics include operational and wide-band amplifiers, gain-bandwidth and power considerations, analysis of noise in integrated circuits, low noise design, feedback, precision passive elements, analog switches, comparators, CMOS voltage references, non-idealities such as matching and supply/IO/substrate coupling.

Text Books:
[1] Allen and Holberg, CMOS Analog Circuit Design, Oxford University Press
[2] Hurst and Meyer, Analysis and Design of Analog Integrated Circuits, Wiley
[3] Behzad Razavi, Design of Analog CMOS ICs, 2000. John Wiley
[4] Jaeger and Blalock, Microelectronics Circuit Design, McGraw Hill

References:
[1] Agarwal & Lang, Foundations of Analog and Digital Electronic Circuits, (The Morgan Kaufmann Series in Computer Architecture and Design)
[2] Behzad Razavi, Introduction to Microelectronics, 2006. John Wiley

DESIGN LAB II			
Course Code:	**EC560**	**Credits:**	**2**
No. of Lab (Hrs/Week):	**3**	**End Sem Exam Hours:**	**3**
Total No. of Lab Sessions:	**10**		

List of Experiments

1. Introduction to Cadence Virtuoso tool and Full Custom IC Design cycle.
2. Realization of an Inverter.
3. Realization of Differential Amplifier.
4. Realization of Common Source Amplifier.
5. Realization of Common Drain Amplifier.
6. Realization of Operational Amplifier.
7. Realization of R-2R DAC.
8. Realization of SAR based ADC.

VLSI FOR WIRELESS COMMUNICATIONS			
Course Code:	**EC408/EC566**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: Introduction
Standards, Communication Systems, Overview of Modulation Scheme, QPSK, BPSK, MSK, Classical Channel, Wireless Channel Description, Path Environment, Path Loss, Friss Equation, Time Varying Channel Models, Envelope Fading, Frequency Selective Fading, Fast Fading.

Unit II: Receiver Architectures
Introduction, Receiver Front: Motivations, Heterodyne and other Architecture, Filter Design: Band Selection Filter, Image Rejection Filter, Channel Filter, Nonidealities and Design Parameters: Nonlinearity, Noise, Derivation of NF, IIP_3 of receiver Front end.

Unit III: Low Noise Amplifier (LNA)
Introduction, Matching Networks, Wideband LNA Design, DC bias, Gain and Frequency Response, Noise Figure, Narrowband LNA, Impedance Matching, Interpretation of Power Matching, Quality Factor, Core Amplifier, Noise Figure, Power Dissipation, Noise Contribution from other sources.

Unit IV: Active Mixers
Unbalanced Mixers, Single Balanced Mixers, Qualitative Description of Gilbert Mixer, Conversion Gain, Distortion analysis of Gilbert Mixer, Comparison of Sample and Hold Circuit and Sampling Mixer.

Unit V: Passive Mixers
Switching Mixers, Distortion in Unbalanced Switching Mixer, Conversion Gain in Unbalanced Switching Mixer, Noise in Unbalanced Switching Mixer, Sampling Mixer, Conversion Gain in Single Ended Sampling Mixer, Distortion in single ended sampling mixer, Intrinsic and Extrinsic noise.

Text Books:
[1] Bosco Leung, "VLSI for Wireless Communication", PHI.

References:
[1] Emad N Farag, M.I Elmasry, "Mixed Signal VLSI Wireless Design Circuits and Systems", Kluwer Publication.
[2] David Tsee, Pramod Viswanath," Fundamentals of Wireless Communication", Cambridge Univ Press.

QUALITY OF SERVICES IN NETWORKS			
Course Code:	**EC406/EC542**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: IP Quality Of Service
Level of QoS, IP QoS history, performance measures, QoS functions, layer 2 QoS technologies, multiprotocol label switching, end-to-end QoS.

Unit II: QOS Architectures
Intserv architecture; RSVP, reservation style, service types, RSVP media support, RSVP scalability, along with their case studies. Diffserv architecture; network boundary traffic conditioners, PHB, resource allocation policy, packet classification.

Unit III: Network Boundary Traffic Conditioners and Resource Allocation
Packet classification, packet marking, need of traffic rate management, traffic policing, traffic shaping along with their case studies. Scheduling of QoS support, sequence number computation based WFQ, flow based WFQ, flow based distributed DWFQ, class based WFQ, priority queuing, schedule mechanisms for voice traffic, MWRR, MDRR along with their case studies.

Unit IV: Congestion Avoidance
TCP slow start and congestion avoidance, TCP traffic behavior in a trial drop scenario, REDproactive queue management for congestion avoidance, WRED, flow WRED, ECN, SPD along with their case studies.

Unit V: QOS in MPLS-Based Networks
MPLS, MPLS with ATM, MPLS QoS, MPLS VPN, MPLS VPN QoS along with their case studies. traffic engineering; MPLS traffic engineering, the layer 2 overlay model, RRR, TE trunk definition, TE tunnel attributes, link resource attributes, distribution of link resource information, path selection policy, TE tunnel setup, link admission control, TE path maintenance, TE RSVP, IGP routing protocols, TE approaches along with their case studies.

Text Books:
[1] Srinivas Vegesna, "IP Quality of Service," CISCO PRESS, 2001.
[2] Santiago alvarez, "Qos for IP/MPLS Networks," Cisco Press, Pearson Education, 2006.

References:
1. IETF website: www.ietf.org

MULTIMEDIA TECHNIQUES			
Course Code:	**CS553/CS653**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit-I: Introduction
Introduction to Multimedia, Multimedia Information, Multimedia Objects, Multimedia in business and work. Convergence of Computer, Communication and Entertainment products.

Stages of Multimedia Projects
Multimedia hardware, Memory & storage devices, Communication devices, Multimedia software's, presentation tools, tools for object generations, video, sound, image capturing, authoring tools, card and page based authoring tools.

Unit-II: Multimedia Building Blocks
Text, Sound MIDI, Digital Audio, audio file formats, MIDI under windows environment Audio & Video Capture.

Unit-III: Data Compression
Huffman Coding, Shannon Fano Algorithm, Huffman Algorithms, Adaptive Coding, Arithmetic Coding Higher Order Modeling. Finite Context Modeling, Dictionary based Compression, Sliding Window Compression, LZ77, LZW compression, Compression, Compression ratio loss less & lossy compression.

Unit-IV: Speech Compression & Synthesis
Digital Audio concepts, Sampling Variables, Loss less compression of sound, loss compression & silence compression.

Unit-V: Images
Multiple monitors, bitmaps, Vector drawing, lossy graphic compression, image file formatting animations Images standards, JPEG Compression, Zig Zag Coding, Multimedia Database .Content based retrieval for text and images, **Video:** Video representation, Colors, Video Compression, MPEG standards, MHEG Standard Video Streaming on net, Video Conferencing, Multimedia Broadcast Services, Indexing and retrieval of Video Database, recent development in Multimedia.

Reference:
[1] Tay Vaughan: Multimedia, Making IT Work, Osborne McGraw Hill.
[2] Buford: Multimedia Systems, Addison Wesley.
[3] Agrawal & Tiwari: Multimedia Systems, Excel.
[4]Mark Nelson: Data Compression Book, BPB.
[5] David Hillman: Multimedia technology and Applications, Galgotia Publications.
[6] Rosch: Multimedia Bible, Sams Publishing.
[7] Sleinreitz: Multimedia System, Addison Wesley.
[8] James E Skuman: Multimedia in Action, Vikas.

SOFT COMPUTING			
Course Code:	**CS551/CS651**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Fuzzy Logic
Introduction to fuzzy logic, classical and fuzzy sets, overview of fuzzy sets, membership function, fuzzy rule generation, operations on fuzzy sets: compliment, intersection, union, combinations on operations, aggregation operation.

UNIT II: Fuzzy Arithmetic
Fuzzy numbers, linguistic variables, arithmetic operations on intervals & numbers, uncertainty based information, information and uncertainty, no specificity of fuzzy and crisp sets, fuzziness of fuzzy sets.

UNIT III: Neural Network
Overview of biological neurons, computational neuron, mathematical model of neurons, ANN architecture, single layer and multilayer architectures, activation function, threshold value, self learning and forced learning algorithms, feed forward and feedback architectures.

UNIT IV: Learning Fundamentals
Learning paradigms, supervised and unsupervised learning, reinforced learning, ANN
training, algorithms perceptions, training rules, delta, back propagation algorithm, multilayer perception model, Hopfield networks, associative memories, applications of artificial neural networks,

UNIT V: Genetic Algorithms
History of genetic algorithm, terminology of genetic algorithm, biological background, creation of offspring, working principles of genetic algorithms, fitness function, reproduction: Roulette wheel selection, Boltzmann selection, cross over mutation, inversion, deletion, and duplication, generation cycle.
Concept of Uncertainty
Presence of uncertainty in real world problems, handling uncertain knowledge, degree of belief, degree of disbelief, uncertainty and rational decisions, decision theory, utility theory, concept of independent events, Bay's rule, using Bay's rule for combining events.

References:
[1] Peteus J. Braspenning: Artificial Neural Networks: An introduction to ANN Theory and Practice, PHI publication, 2005.
[2] Paul P. Wang: Fuzzy Logic: A spectrum of Theoretical and Practical issues, Pearson publication 2004.
[3] Lotfi Asker Zadeh, George J. Kilr, Bo Yuan Fuzzy: Sets, Fuzzy logic, and Fuzzy Systems: Selected Papers-, 2005.
[4] Foundations of Fuzzy logic and Soft Computing: 12th International Fuzzy conference proceeding, 2005.
[5] Particia Melin: Neural Networks Theory, Oxford University press, 2003
[6] Oscar Castillo: Neural Networks Theory and Application, Wiley Eastern publication 2003.

WIRELESS SYSTEM DESIGN			
Course Code:	**EC534**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I:
RF system design procedures, methodology, link budget, propagation models, tower-top amplifiers, RF design guidelines, traffic projections, cell site design,

Unit II:
Network design- traffic forecasts, node dimensioning, interface design, placement of network nodes, topology

Unit III:
Antenna systems,-base station antenna, cross pole antenna, dual band antenna, intelligent antenna, diversity techniques-derivation of selection diversity and maximal ratio combining improvement, polarization diversity, frequency diversity, time diversity, RAKE receiver

Unit IV:
UMTS system design-design principles, coverage analysis, capacity analysis, radio access networks, overloading UMTS over GSM, CDMA system design-design methodology, deployment guidelines, traffic estimation, radio elements, fixed network d4sign requirements, traffic models, link budget, case studies-CDAM2000 1xRTT, EVDO, CDMA2000 1xRTT with EVDO overlay

Unit V:
Communication sites-types, installation, towers, stealth, in-building and tunnel systems, inter, modulation, collocation, Study of various network simulators, GloMoSim, ns-2, Opnet, designing and evaluating performance of transport and routing protocols of mobile and wireless networks.

Text Books:
[1] Clint Smith, P.E. Daniel Collins: 3G Wireless Networks" Tata McGraw-Hill, 2nd Edition
[2]Theodore S. Rappaport: Wireless Communication, Principles and Practice" Pearson

References:
IEEE Journals and proceedings

OPEN SOURCE SOFTWARE SYSTEM			
Course Code:	**CS404/CS534**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Open Source Software (OSS)

History, philosophy, ethics, licensing, Pernes' principle, open source software methodology, open source vs. closed source, open source software vs. free software, open source software vs. source available, Windows and Linux, open source standards, open source development environment, OSS in e-government, OSS management, OSS management tools: taskjuggler, dotProject.net, licenses, open source content management system, project management via open source and open standard, copyright, patent, social dynamic of collaboration and legal implication of software intellectual property.

UNIT II: Open Source Technology and Infrastructure

Operating system: Linux, Berkeley Software Distribution (BSD); protocols: low level protocols, high level protocols; common open source language: presentation language, system programming languages, scripting languages; database system: MYSQL, PostgreSQL, BerkeleyDB; web services: Apache; communication servers: send mail, jabber; application and messaging server: Open3.org, Enhydra.org, JBoss, Zope, Zend, Open Source Desktop and server Applications.

UNIT III: Open Source Standards

Standards, open standards, benefits of open standards, national considerations, standard setting organization and processes, open standard organization for internet networking and application/services, computer graphics and multimedia, office documents, open standards usage, Linux standard base, Linux standard base as an ISO standard, Linux standards base certification, patents in standards.

UNIT IV: Open Source Software Applications

Rapid web application development framework: Ruby on Rail (ROR), Model-View-Controller (MVC) model, Don't Repeat Yourself (DRY) principle, convention over configuration principle, open source applications - business applications: Enterprise Resource Planning (ERP), Customer Relationship Management (CRM); educational applications: educational suites, learning support, language,; groupware: Content Management Systems (CSM), Wiki software; programming language support: bug trackers, code generators, configuration software.

UNIT V: Open Source in the Enterprise

Modern era of open source, rebranding open source, character of the community, open source community development, open source and enterprise applications, risks and benefits of using open source in the enterprise, developing an enterprise application strategy, cost, licensing and resources of OSS.

References:

[1] O'Reilly Media, Dan Woods: Open Source for the Enterprise: Managing Risks, Reaping Rewards,, 2005.
[2] James Lee, Brent Ware: Open Source Web Development with LAMP, Pearson Education, 2008.
[3] Paul Kavanagh: Open Source Software: Implementation and Management, Digital Press, 2004.
[4] Steven Weber: The Success of Open Source, Harvard University Press, 2004.

DESIGN OF SEMICONDUCTOR MEMORIES			
Course Code:	**EC568**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: RAM Technologies

Static Random Access Memories (SRAMs): SRAM Cell Structures-MOS SRAM Architecture-MOS SRAM Cell and Peripheral Circuit Operation-Bipolar SRAM Technologies, Application Specific SRAMs. Dynamic Random Access Memories (DRAMs): DRAM Technology Development-CMOS DRAMs, DRAMs Cell Theory

UNIT II: Non Volatile Memories
Masked Read-Only Memories, High Density ROMs, PROMs, CMOS PROMs, EEPROMs, Floating-Gate EPROM Cell, Electrically Erasable PROMs, EEPROM Technology And Architecture, Nonvolatile SRAM, Flash Memories, Advanced Flash Memory Architecture.

UNIT III: Memory Testing
RAM Fault Modeling, Electrical Testing, Pseudo Random Testing-Megabit DRAM Testing-Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing- Application Specific Memory Testing.

UNIT IV: Reliability and Radiation Effects
General Reliability Issues, RAM Failure Modes and Mechanics, Nonvolatile Memory Reliability, Reliability Modeling and Failure Rate Prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and Qualification, RAM Fault Modeling, Electrical Testing, Psuedo Random Testing, Megabit DRAM Testing, Nonvolatile Memory Modeling.

UNIT V: Packaging Technologies
Radiation Effects, Single Event Phenomenon, Radiation Hardening Techniques, Radiation Hardening Process and Design Issues, Radiation Hardened Memory Characteristics, Radiation Hardness Assurance and Testing, Radiation Dosimeter, Water Level Radiation Testing and Test Structures. Ferroelectric Random Access Memories, GaAs FRAMs, Analog Memories, Magnetoresistive Random Access Memories

Text Books:
[1] Ashok K. Sharma: Semiconductor Memories Technology, Testing and Reliability, Prentice-Hall of India Private Limited, New Delhi, 1997.
[2] Tegze P. Haraszti: CMOS Memory Circuits, Kluwer Academic publishers, 2001.

PRINCIPLES OF MEMS DESIGN			
Course Code:	**EC570**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Introduction to MEMS
MEMS and Microsystems, Miniaturization, Typical products, Micro sensors, Micro actuation, MEMS with micro actuators, Micro-accelerometers and Micro fluidics, MEMS materials, Micro fabrication

UNIT II: Mechanics for MEMS Design
Elasticity, Stress, strain and material properties, Bending of thin plates, Spring configurations, torsional deflection, Mechanical vibration, Resonance, Thermo mechanics – actuators, force and response time, Fracture and thin film mechanics.

UNIT III: Electrostatic Design
Electrostatics: basic theory, electro static instability. Surface tension, gap and finger pull up, Electro static actuators, Comb generators, gap closers, rotary motors, inch worms, Electromagnetic actuators. bistable actuators.

UNIT IV: Circuit and System Issues
Electronic Interfaces, Feedback systems, Noise, Circuit and system issues, Capacitive Accelerometer, Piezoelectric pressure sensor, Modeling of MEMS systems, CAD for MEMS.

UNIT V: Introduction to Optical and RF MEMS
Optical MEMS, - System design basics – Gaussian optics, matrix operations, resolution. Case studies, MEMS scanners and retinal scanning display, Digital Micro mirror devices. RF Memes – design basics, case study – Capacitive RF MEMS switch, performance issues.

Text Books:
[1] Stephen Santuria: Microsystems Design, Kluwer publishers, 2000.
[2] Nadim Maluf: An introduction to Micro electro mechanical system design, Artech House, 2000.

References:
[1] Mohamed Gad-el-Hak: The MEMS Handbook, CRC press Baco Raton,2000.
[2] Tai Ran Hsu: MEMS & Micro systems Design and Manufacture Tata McGraw Hill, New Delhi, 2002.

SOLID STATE ELECTRONICS DEVICES			
Course Code:	**EC572**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Fundamental Models
Physical models-bohr model, quantum mechanics, atomic structure, energy bands & charge carriers in semi conductors, carrier concentration, drift of carriers in electric and magnetic fields, diffusion of carriers. Continuity equation. Semi-conductor materials. Introduction to solid state electronics.

UNIT II: Diodes
Fabrication of P-N junctions, equilibrium conditions, forward and reverse biased junctions, steady state conditions, reverse bias breakdown, transient and a.c. condition, Recovery time, deviation from simple theory, metal semi-conductor junction, heterojunction. P-N junction linearly graded and step junction diodes, tunnel diode, photo diode, light emitting diodes and lasers.

UNIT III: BJTs
BJT amplification & switching: Fundamental of BJT operation, minority carier distribution & terminal currents, generalized biasing, switching, frequency limitation of transistors, ebber Molls model, Gummel Poon Model of BJTs. Heterojuction bipolar transistor.

UNIT IV: FETs
FET-metal semi-conductor (MESFETs), FET-Metal insulator semiconductor (MOSFET). Power MOSFETs, MODFETs, High Electron Mobility Transistors.

UNIT V: Integrated circuits
Monolithic device elements, charge transfers devices, very large scale integration, testing of VLSI chips, Stuck at faults and Fault diagnosis.

Text Book:
[1] Ben G Streetman, Solid State Electronic Devices PHI
References:
[1] S M Sze: Physics of semiconductor Devices, Wiley Pub.
[2] Kittel C: Introduction to Solid State Physics, Wiley Pub.

INTEGRATED CIRCUIT PHYSICAL DESIGN			
Course Code:	**EC574**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: The Well
Substrate, Parasitic Diode, N-well as a Resistor, N-well patterning and layout, Design Rules, Resistance calculation, N-well Resistor, N-well/Substrate Diode, Carrier Concentrations, Fermi Energy Level, Depletion Layer Capacitance, Storage or Diffusion Capacitance, RC Delay through the N-well, Distributed RC Delay, Distributed RC Rise Time, Twin Well Processes.

Unit II: The Metal Layers
Bonding Pad and layout, Metal-to-Substrate capacitance, Passivation, Design and Layout of Metal Layers, Metal1 and Via1, Parasitic Associated with Metal Layers, Intrinsic Propagation Delay, Current-Carrying Limitations, Design Rules for Metal Layers, Contact Resistance, Crosstalk and Ground Bounce , Crosstalk, Ground Bounce, DC Problems, AC Problems.

Unit III: The Active and Poly Layers
Layout Using Active and Poly Layers, P- and N-Select Layers, Poly Layer, Self-Aligned Gate, Poly Wire, Silicide Block, Connecting Wires to Poly and Active, Connecting P-Substrate to Ground, N-Well Resistor layout, NMOS and PMOS Device layout, Standard Cell Frame, Design Rules, Electrostatic Discharge (ESD) Protection, Diodes layout.

Unit IV: Resistors, Capacitors, MOSFETs
Resistors, Temperature Coefficient, Voltage Coefficient, Unit Elements, Guard Rings, Interdigitated Layout, Common- Centroid Layout, Dummy Elements, Poly-Poly Capacitor layout, Parasitic, MOSFETs: Lateral Diffusion, Oxide Encroachment, Source/Drain Depletion Capacitance, Source/Drain Parasitic Resistance, Long-Length MOSFETs layout, Large-Width MOSFETs layout, MOSFET Capacitances.

Unit V: MOSFET Operation
Accumulation, Depletion, Strong Inversion, Threshold Voltage, Characteristics of MOSFETs, MOSFET Operation: Triode and Saturation, Cgs Calculation, Long-Channel MOSFET Models, Model Parameters Related to the Drain Current, Modeling of the Source and Drain Implants Short-Channel MOSFETs Hot Carriers, Lightly Doped Drain, MOSFET Scaling, Short-Channel Effects, Oxide Breakdown, Drain-Induced Barrier Lowering, Gate-Induced Drain Leakage.

Text Books:
[1] R. Jacob Baker: CMOS Circuit Design, Layout, and Simulation, Second Edition.
[2] Christopher Saint, Judy Saint: IC Layout Basics: A Practical Guide

References:
[1] Dan Clein: CMOS IC Layout : Concepts, Methodologies, and Tools,.
[2] Alan Hastings, Roy Alan Hastings: The Art of Analog Layout

CMOS RF CIRCUIT DESIGN			
Course Code:	**EC576**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Introduction to RF design and Wireless Technology
Design and Applications, Complexity and Choice of Technology. Basic concepts in RF design: Nonlinearly and Time Variance, Intersymbol interference, random processes and noise. Sensitivity and dynamic range, conversion of gains and distortion.

UNIT II: RF Modulation
Analog and digital modulation of RF circuits, Comparison of various techniques for power efficiency, Coherent and non-coherent detection, Mobile RF communication and basics of Multiple Access techniques, Receiver and Transmitter architectures, Direct conversion and two-step transmitters.

UNIT III: RF Testing
RF testing for heterodyne, Homodyne, Image reject, Direct IF and sub sampled receivers.

UNIT IV: BJT and MOSFET Behavior at RF Frequencies
BJT and MOSFET behavior at RF frequencies, modeling of the transistors and SPICE model, Noise performance and limitations of devices, integrated parasitic elements at high frequencies and their monolithic implementation

UNIT V: RF Circuits Design
Overview of RF Filter design, Active RF components & modeling, Matching and Biasing Networks. Basic blocks in RF systems and their VLSI implementation, Low noise Amplifier design in various technologies, Design of Mixers at GHz frequency range, Mixers- working and implementation. Oscillators- Basic topologies VCO and definition of phase noise, Noise power and trade off. Resonator VCO designs, Quadrature and single sideband generators. Radio frequency Synthesizers- PLLS, Various RF synthesizer architectures and frequency dividers, Power Amplifier design, Liberalization techniques, Design issues in integrated RF filters.

Text Book:
[1] Thomas H. Lee: Design of CMOS RF Integrated Circuits, Cambridge University press 1998.

References:
[1] B. Razavi: RF Microelectronics, PHI, 1998
[2] R. Jacob Baker, H.W. Li, D.E. Boyce CMOS Circuit Design, layout and Simulation PHI, 1998
[3] Y.P. Tsividis: Mixed Analog and Digital Devices and Technology, TMH, 1996

CMOS VLSI DESIGN			
Course Code:	**EC578**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: MOS Transistor theory
nMOS / pMOS transistor, threshold voltage equation, body effect, MOS device design equation, sub threshold region, Channel length modulation. mobility variation, Tunneling, punch through, hot electron effect MOS models, small signal AC Characteristics, CMOS inverter, βn / βp ratio, noise margin, static load MOS inverters, differential inverter, transmission gate, tristate inverter, BiCMOS inverter.

UNIT II: CMOS Process Technology
Lambda Based Design rules, scaling factor, semiconductor Technology overview, basic CMOS technology, p well / n well / twin well process. Current CMOS enhancement (oxide isolation, LDD. refractory gate, multilayer inter connect) , Circuit elements, resistor , capacitor, interconnects, sheet resistance & standard unit capacitance concepts delay unit time, inverter delays , driving capacitive loads, propagate delays, MOS mask layer, stick diagram, design rules and layout, symbolic diagram, mask feints, scaling of MOS circuits.

UNIT III: Basics of Digital CMOS Design
Combinational MOS Logic circuits-Introduction, CMOS logic circuits with a MOS load, CMOS logic circuits, complex logic circuits, Transmission Gate. Sequential MOS logic Circuits - Introduction, Behavior of hi stable elements, SR latch Circuit, clocked latch and Flip Flop Circuits, CMOS D latch and triggered Flip Flop. Dynamic Logic Circuits - Introduction, principles of pass transistor circuits, Voltage boot strapping synchronous dynamic circuit techniques, Dynamic CMOS circuit techniques.

UNIT IV: CMOS Analog Design
Introduction, Single Amplifier. Differential Amplifier, Current mirrors, Band gap references, basis of cross operational amplifier.

UNIT V: Dynamic CMOS and clocking
Introduction, advantages of CMOS over NMOS, CMOS\SOS technology, CMOS\bulk technology, latch up in bulk CMOS, static CMOS design, Domino CMOS structure and design, Charge sharing, Clocking-clock generation, clock distribution, clocked storage elements.

Text Books:
[1] Neil Weste and K. Eshragian: Principles of CMOS VLSI Design: A System Perspective, 2nd edition, Pearson Education (Asia) Pte. Ltd., 2000.
[2] Wayne, Wolf: Modern VLSI design: System on Silicon, Pearson Education, 2nd Edition

References:
[1] Douglas A Pucknell & Kamran Eshragian: Basic VLSI Design, PHI, 3rd Edition
[2] Sung Mo Kang & Yosuf Lederabic Law: CMOS Digital Integrated Circuits: Analysis and Design, McGraw-Hill, 3rd Edition

VLSI DESIGN TECHNIQUES			
Course Code:	**EC580**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: MOS Transistor Theory and Process Technology
NMOS and PMOS transistors, Threshold voltage- Body effect- Design equations- Second order effects. MOS models and small signal AC characteristics. Basic CMOS technology.

UNIT II: Inverters and Logic Gates
NMOS and CMOS Inverters, Stick diagram, Inverter ratio, DC and transient characteristics , switching times, Super buffers, Driving large capacitance loads, CMOS logic structures , Transmission gates, Static CMOS design, dynamic CMOS design.

UNIT III: Circuit Characterization and Performance Estimation
Resistance estimation, Capacitance estimation, Inductance, switching characteristics, transistor sizing, power dissipation and design margining. Charge sharing ,Scaling.

UNIT IV: VLSI System Components Circuits and System Level Physical Design
Multiplexers, Decoders, comparators, priority encoders, Shift registers. Arithmetic circuits – Ripple carry adders, Carry look ahead adders, High-speed adders, Multipliers. Physical design – Delay modeling ,cross talk, floor planning, power distribution. Clock distribution.

UNIT V: Verilog Hardware Description Language
Overview of digital design with Verilog HDL, hierarchical modeling concepts, modules and port definitions, gate level modelling, data flow modeling, behavioral modeling, task & functions, Test Bench.

Text Books:
[1] Neil H.E. Weste and Kamran Eshraghian: Principles of CMOS VLSI Design, Pearson Education ASIA, 2nd edition, 2000.
[2] John P.Uyemura: Introduction to VLSI Circuits and Systems, John Wiley & Sons, Inc., 2002.
[3] Samir Palnitkar: Verilog HDL, Pearson Education, 2nd Edition, 2004.

References:
[1] Eugene D.Fabricius: Introduction to VLSI Design McGraw Hill International Editions, 1990.
[2] J.Bhasker, B.S.Publications: A Verilog HDL Primer, 2nd Edition, 2001.
[3] Pucknell: Basic VLSI Design, Prentice Hall of India Publication, 1995.
[4] Wayne Wolf: Modern VLSI Design System on chip, Pearson Education, 2002

ADVANCED RF ENGINEERING			
Course Code:	**EC544**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Introduction to RF Electronics
Introduction to RF Design and Wireless Technology: Design and Applications,

UNIT II: Complexity and Choice of Technology
Basic concepts in RF design: Nonlinearly and Time Variance, Inter symbol interference, random processes and noise. Sensitivity and dynamic range, conversion of gains and distortion

UNIT III: RF Modulation
Analog and digital modulation of RF circuits, Comparison of various techniques for power efficiency, Coherent and non-coherent detection, Mobile RF communication and basics of Multiple Access techniques. Receiver and Transmitter architectures, direct conversion and two-step transmitters. RF Testing: RF testing for heterodyne, Homodyne, Image reject, Direct IF and sub sampled receivers.

UNIT IV: BJT and MOSFET Behavior at RF Frequencies
BJT and MOSFET behavior at RF frequencies, modeling of the transistors and SPICE model, Noise performance and limitations of devices, integrated parasitic elements at high frequencies and their monolithic implementation Overview of RF Filter design, Active RF components & modeling,

UNIT V: RF Circuits Design
Matching and Biasing Networks. Basic blocks in RF systems and their VLSI implementation, Low noise Amplifier design in various technologies, Design of Mixers at GHz frequency range, Various mixers- working and implementation. Oscillators- Basic topologies VCO and definition of phase noise, Noise power and trade off. Resonator VCO designs, Quadrature and single sideband generators. Radio frequency Synthesizers- PLLS, Various RF synthesizer architectures and frequency dividers, Power Amplifier design, Liberalization techniques, Design issues in integrated RF filters.

Text books:
[1] B. Razavi: RF Microelectronics, PHI, 1998
[2] R. Jacob Baker, H.W. Li, D.E. Boyce: CMOS Circuit Design, layout and Simulation, PHI, 1998.

References:
[1] Thomas H. Lee: Design of CMOS RF Integrated Circuits, Cambridge University Press, 1998.
[2] Y.P. Tsividis: Mixed Analog and Digital Devices and Technology, TMH, 1996
[3] David M. Pozar: Microwave Engineering, John Wiley & Sons, 2nd Edition, 2003.

PROBABILITY AND STOCHASTIC PROCESSES			
Course Code:	**EC548**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I:
Probability models, Algebra of events, probability axioms, conditional probability, Baye's rules, Bernoulli traits. **Discrete Random Variables**: Discrete random variables, probability mass functions, discrete distribution functions-Bernoulli, Binomial, geometric, Poisson, hyper geometric & uniform distributions, probability generating function.

Unit II:
Continuous Random variable: Exponential distribution, memory less property, application to reliability, hypo exponential, Erlang, Gamma, hyper exponential & Normal distributions ,order statistics, distribution of sums.

Unit III:
Stochastic Process, Classification, Discrete and continuous time markov chain, Poisson process, renewal process, littles's formula, Erlang Loss Model, M/M/1 Queue, M/M/m Queue Multidimensional Queue.

Unit IV:
Solution Techniques: Steady-State Solutions of Markov Chains, Solution for a Birth Death Process, Matrix-Geometric Method: Quasi-Birth-Death Process, Heisenberg Matrix: Non-Markovian Queues, Transient analysis, stochastic Petri nets, Numerical Solution: Direct Methods, Numerical Solution: Iterative Methods, Comparison of Numerical Solution Methods, Performance Measures,

Unit V:
Queueing Networks. Definitions and Notation. Performance Measures. Product-Form Queueing Networks. Algorithms for Product-Form Networks, priority Networks.

Reference Books:
[1] Research Methodologies, R. Panneerselvam, Prentice Hall, 2007.
[2] Research in Education, Best John V. and James V Kahn, Wiley eastern, 2005.
[3] Elements of Educational Research, Sukhia, S.P., P.V. Mehrotra, and R.N. Mehrotra, PHI publication, 2003.
[4] Methodology of Research Education, K. Setia, IEEE publication, 2004.
[5] Research methodology, Methods and Techniques, Kothari, C.R., 2000.

ADVANCED MICROWAVE COMMUNICATION			
Course Code:	**EC550**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Microwave and Millimeter Wave Devices
Overview of microwave and millimeter wave vacuum tube devices, limitations of microwave vacuum tubes, gyratron vacuum tube devices. Advances in microwave and millimeter wave solid state devices, Gunn devices, oscillator using, Gunn diode, and injection locked oscillators, IMPATT devices, and microwave and mm wave performance of IMPATT. Other solid state devices like Tunnel diode, BARITT and TRAPAT. Microwave and mm wave circuits.

UNIT II: Microwave and MM Wave Circuits
Review of scattering matrix concept in the light of vector network analyzer, impedance matching network, couplers, power dividers, resonators and filters, Detectors, mixers, attenuators, phase shifters, amplifier and oscillator, Ferrite based circuits.

UNIT III: Antennas
Hertzian dipole, loop antenna, helical antenna, frequency independent antenna: Du0Hamel principle, log spiral and log periodic dipole antenna array. Babinet principle, waveguide slot antenna, microstrip antenna, horn antenna, parabolic reflector. Antenna arrays and phased array antenna.

UNIT IV: Satellite Communication
Orbital parameters, satellite trajectory, period, geostationary satellites, non-geostationary constellations. Communication satellites – Space craft subsystems, payload – repeater, antenna, attitude and control systems, telemetry, tracking and command, power sub system and thermal control. Earth stations antenna and feed systems, satellite tracking system, amplifiers, fixed and mobile satellite service earth stations. Terrestrial: line of sight transmission, relay towers and distance considerations. Communication link design: Frequency bands used, antenna parameters, transmission equations, noise considerations, link design, propagation characteristics of fixed and mobile satellite links, channel modeling, very small aperture terminals (VSAT), VSAT design issues.

UNIT V: Microwave and MM Wave Propagation.
Overview of basic radio wave propagation mechanisms, Friis transmission formula, plane earth propagation model, troposcatter systems, ionosphere propagation, duct propagation, microwave radio link and calculation of link budget. Effect on radio wave propagation due to rain, fog, snow, ice, atmospheric gases, Earth's magnetic field.

Text Books:
[1] David M Pozar: Microwave Engineering, John Wiley & Sons
[2] R E Collin, Antenna & Radio wave Propagation, McGraw Hill Book Co.

References:
[1] M Richharia: Satellite Communication Systems,2nd Edition, Macmillan Press Ltd.
[2] Ferdo Ivanek: Terrestrial Digital Microwave Communications, Artech House
[3] E. Hund: Microwave Communications, IEEE Press
[4] Jordan & Balman: Electromagnetic waves & Radiating System
[5] R E Collin: Microwave Engineering, McGraw Hill Co.

IMAGE PROCESSING AND BIOMETRICS			
Course Code:	**EC418/EC556**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: Image Processing and Image Enhancement
Introduction, An image model, sampling & quantization, Basic relationships between Pixels, imaging geometry, Properties of 2 – D Fourier transform, FFT algorithm and other separable image transforms, Components of an image processing System., Digital Image Fundamentals- elements of visual perception, image sensing and acquisition, Basic relationships between pixels
Fundamentals of spatial filtering, smoothing spatial filters (linear and non-linear).

Unit II: Pattern Recognition
Fundamentals of Pattern Recognition, Recognition Measurement, Errors, and Statistics, Recognition measurement and testing, Identification System Errors and Performance Testing, Computer Security, Bayesian decision theory, Multilayer neural networks, Unsupervised Learning and Clustering.

Unit III: Biometrics
Introduction to Biometrics, Fingerprints: Ridges, Furrows, Types of Fingerprints, Image and Signal Processing, Biometric Signal Processing, Other Biometric Modalities, Comparing Biometrics, Passwords, and Tokens, Multimodal Biometrics, Biometric Resources and Standards, Large Scale Biometrics and Systems Case Studies.

Unit IV: Analysis in Biometrics
Large-Scale Biometric Identification: Challenges and Solutions, Issues Involving the Human Biometric Sensor Interface, Fundamentals of Biometric-Based Training System Design, Biometric Systems and Applications, Force Field Feature Extraction for Fingerprint Biometrics, Behavioral Biometrics for Online Computer User Monitoring.

Unit V: Synthesis in Biometrics:
Introduction to Synthesis in Biometrics, Local B-Spline Multiresolution with Example in Iris Synthesis and Volumetric Rendering, image smoothing filters (Butterworth and Guassian low pass filters), image sharpening filters (Butterworth and Guassian high pass filters), selective filtering, Computational Geometry and Image Processing in Biometrics: On the Path to Convergence, **,** A Statistical Model for Biometric Verification.

Text Books:
[1] Practical Algorithms for Image Analysis: Description, Examples, and Code, Seul, O'Gorman, Sammon, 2000.
[2] S. Annadurai and R. Shanmugalakshmi: Fundamentals of Digital Image Processing, Pearson Education.
[3] R. C. Gonzalez and R. E. Woods: Digital Image Processing, 3rd Edition, Pearson Education.
[4] A. K. Jain: Fundamentals of Digital Image Processing, PHI Learning.
References:
[1] M. Sonka, V. Hlavac and R. Boyle: Digital Image Processing and Computer Vision: Cengage Learning.
[2] B. Chanda and D. D. Majumder: Digital Image Processing and Analysis, PHI Learning.
[3] S. Jayaraman, S. Esakkirajan and T. Veerakumar: Digital Image Processing, TMH.

ADVANCED COMMUNCIATION NETWORKS			
Course Code:	**EC402/EC532**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: Digital switching systems-analysis, hierarchy, evolution, SPC, call processing, communication and control- level 1,2,& 3 control, interface control, network control processor, central processor, control architecture, multiplexed highways, switching fabric-space division switching, time division switching, STS, TST, TTT, switching system software-architecture, OS, database management

Unit II: MPLS-label stack and label distribution, traffic engineering, design of switching systems, and routers, switching networks-crossbar switches, multistage switches, shared memory switches, optical networks, DWDM techniques, IP over optical core switches

Unit III: Congestion control: integrated services, differentiated services, congestion control, congestion control in packet switching, frame relay congestion control, flow control at link level, TCP congestion control

Unit IV: Voice over IP: basic IP telephone system, digital voice sampling, compression techniques, protocol for VoIP, session initiation protocol

Unit V: Internetworking-connection mode network service, x.75 internetworking, network through ISDN, internetworking SNA, and x.25, x.300 internetworking standards, personal computer networking, data transmission in PTN, Data network standards, voice-data integration, fast packet switches

Text books:

[1] Syed R. Ali, " Digital Switching Systems, System Reliability and analysis, Tata McGraw-Hill
[2] William Stallings, " High Speed Networks and Internet" 2nd ed. Perason edu, 2005
[3] Bellamy John, " Digital Telephony" Wiley 3rd Ed, 2000
[4] Viswanathan, T, "Telecommunications Switching Systems and Networks, " PH

References:

[1] Andrew S. Tanenbaum: Computer networks, PHI.
[2] W. Stallings: Data and computer communications, MC, Milan.
[3] Alberto Leon-Gercia, India Widjaja: Communication networks, fundamental concepts and key architecture, TATA McGraw Hill.
[4] Bertsekas D. and Gallager R.: Data Networks, PHI.
[5] Keshav S: An Engineering Approach to computer Networking, Addison Weslay.

LOW POWER VLSI DESIGN			
Course Code:	**EC633**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Introduction
Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches. Physics of power dissipation in CMOS devices.

UNIT II: Device & Technology Impact on Low Power
Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation.

UNIT III: Power estimation
Simulation Power analysis: SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, data correlation analysis in DSP systems. Monte Carlo simulation. Probabilistic power analysis: Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.

UNIT IV: Low Power Design
Circuit level: Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library. Logic level: Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic.

UNIT V: Low power Architecture & Systems
Power & performance management, switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design. Low power Clock Distribution: Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip & package co design of clock network. Algorithm & architectural level methodologies: Introduction, design flow, Algorithmic level analysis & optimization, Architectural level estimation & synthesis.

Text Books:
[1] Gary K. Yeap: Practical Low Power Digital VLSI Design, KAP, 2002
[2] Rabaey and Pedram: Low power design methodologies, Kluwer Academic, 1997

References :
[1] Kaushik Roy, Sharat Prasad: Low-Power CMOS VLSI Circuit Design, Wiley, 2000
[2] J. B. Kulo and J.H Lou: Low voltage CMOS VLSI Circuits, Wiley 1999.
[3] A.P. Chandrasekaran and R.W. Broadersen: Low power digital CMOS design, Kluwer, 1995.
[4] Abdelatif Belaouar, Mohamed.I. Elmasry, "Low power digital VLSI design, Kluwer, 1995.

DESIGN LAB III			
Course Code:	**EC683**	**Credits:**	**2**
No. of Lab (Hrs/Week):	**3**	**End Sem Exam Hours:**	**3**
Total No. of Lab Sessions:	**10**		

List of Experiments

1. Introduction to simulation software ANSYS using GUI.
2. Introduction to simulation software ANSYS using Command lines.
3. Performing a Harmonic Response Analysis using ANSYS.
4. Realization of a Force Sensor using ANSYS.
5. Multiplysics Analysis of a Thermal Actuator using ANSYS.
6. Piezoelectric Analysis using ANSYS.
7. Introduction to MEMS Design using ANSYS.
8. Electromechanical Analysis of an Optical Brag Reflector using ANSYS.

RESEARCH TECHNIQUES IN ICT			
Course Code:	**CS633**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I : Introduction to Research Techniques
Meaning of research, objectives of research, motivation in research, types of research-Introduction to experimental test bed, algorithmic research, simulation research, mathematical modeling approach, characteristics and prerequisites of research, significance of research, research process, Sources of research problem, criteria of identifying the problem, necessity of defining the problem, errors in selecting research problem, technique involved in defining the problem, Report and paper writing

Unit II: Data Analysis and Statistical Techniques
Data and their analyses, quantitative methods and techniques, Measure of central tendency, measures of variation, frequency distribution, analysis of variance methods, identifying the distribution with data, parameter estimation, Goodness-of-Fit tests-Chi-Square test, K-S Goodness-of-Fit test, Correlation analysis, Regression analysis, time series and forecasting, Introduction to discriminant analysis, factor analysis, cluster analysis, conjoint analysis. Sampling methods, test of hypothesis.

Unit III: Random Numbers and Variates
Properties of random numbers, generation, tests for random numbers, random-variate generation
Inverse Transform technique, direct transformation, convolution method, acceptance-rejection Technique, Probability distributions functions, Moments, moment generating functions, joint distributions, marginal and conditional distributions, functions of two dimensional random variables Poisson process-Markovian queues, single and multi server models, Little's formula, steady state analysis

Unit IV: Algorithmic Research
Algorithmic research problems, types of algorithmic research, types of solution procedure, steps of development of algorithm, steps of algorithmic research, design of experiments,

Unit V: Simulation and Soft Computing Techniques
Introduction to soft computing, Artificial neural network, Genetic algorithm, Fuzzy logic and their applications, Tools of soft computing, Need for simulation, types of simulation, simulation language, fitting the problem to simulation study, simulation models, verification of simulation models, calibration and validation of models, Output analysis, introduction to MATLAB, NS2, ANSYS, Cadence

Text Books:
[1] R. Panneerselvam: Research Methodologies, PHI
[2] Jerry Banks, John S. Carson, Barry.L. Nelson David. M. Nicol: Discrete-Event System Simulation, Prentice-Hall India
[3] Donald Gross, Carl M. Harris: Fundamentals of Queueing Theory, 2nd Ed. John Wiley and Sons, New York,

References:
[1] Best John V. and James V Kahn: Research in Education, Wiley eastern, 2005.
[2] Sukhia, S.P., P.V. Mehrotra, and R.N. Mehrotra: Elements of Educational Research, PHI publication, 2003.
[3] K. Setia: Methodology of Research Education, IEEE publication, 2004.
[4] Kothari, C.R.: Research methodology, Methods and Techniques, 2000.

MICRO AND SMART SYSTEM TECHNOLOGY			
VLSI ASIC DESIGN			
Course Code:	**EC665**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I : Introduction to ASICs, CMOS Logic and ASIC Library Design
Types of ASICs - Design flow - CMOS transistors CMOS Design rules - Combinational Logic Cell – Sequential logic cell - Data path logic cell - Transistors as Resistors – Transistor Parasitic Capacitance- Logical effort –Library cell design - Library architecture.

UNIT II: Programmable ASICs, Programmable ASIC Logic Cells and ASICs I/O Cells.
Anti fuse - static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX DC & AC inputs and outputs - Clock & Power inputs - Xilinx I/O blocks.

UNIT III: Programmable ASIC Interconnect, Programmable ASIC Design Software and Low Level Design Entry
Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 – Altera FLEX –Design systems - Logic Synthesis - Half gate ASIC -Schematic entry - Low level design language - PLA tools -EDIF- CFI design representation.

UNIT IV: Logic Synthesis, simulation and Testing
Verilog and logic synthesis -VHDL and logic synthesis - types of simulation- boundary scan test - fault simulation - automatic test pattern generation.

UNIT V: ASIC Construction, Floor Planning, Placement and Routing
System partition, FPGA partitioning, partitioning methods, floor planning, placement, physical design flow, global routing, detailed routing, special routing, circuit extraction, DRC.

Text Books:
[1] M.J.S .Smith, Application Specific Integrated Circuits, Addison -Wesley Longman Inc., 1997.
[2] Farzad Nekoogar and Faranak Nekoogar, From ASICs to SOCs: A Practical Approach, Prentice Hall PTR, 2003.

References:
[1] Wayne Wolf, FPGA-Based System Design, Prentice Hall PTR, 2004.
[2] R. Rajsuman, System-on-a-Chip Design and Test. Santa Clara, CA: Artech House, 2000.

Course Code:	**EC667**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT 1: Introduction to Micro and Smart Systems
Smart-material systems, Evolution of smart materials, structures and systems, Components of a smart system, Application areas, Commercial products, Microsystems, Feynman's vision, Micromachined transducers, Evolution of micro-manufacturing, Applications.

UNIT II: Micro and Smart Devices and Systems: Principles and Materials:
Microsensors, silicon capacitive accelerometer, resonant accelerometer, piezo-resistive pressure sensor, capacitive pressure sensor, inertial sensor, sensor for munitions, microresonator, tunable rf filters, actuators, , microvalve/micropumps, microactuator, microgripper, detectors, flow sensor, accelerometer, gyros sensor, enhanced jet engine, chemical sensor, biosensors, DNA chips, micro thruster, CNT.

UNIT III: Micromanufacturing and Material Processing
Materials: types, mechanical properties, electronics properties and optical properties. Processing of other materials: ceramics, polymers and metals, silicon wafer processing, lithography, nanolithography, micro contact printing lithography, thin-film deposition, etching (wet and dry), TMAH etching, LIGA, laser ECE, wafer-bonding, and metallization, Silicon micromachining: surface, bulk, moulding, bonding based process flows, Thick-film processing, Smart material processing, Emerging trends.

UNIT IV: Modeling, Design and Simulations
Scaling issues, Elastic deformation and stress analysis of beams and plates, Residual stresses and stress gradients, Thermal loading, Heat transfer issues, Basic fluids issues, Electrostatics. Coupled electromechanics. Electromagnetic actuation, Capillary electro-phoresis. Piezoresistive modeling, Piezoelectric modeling. Magnetostrictive actuators,finite element method overview.

UNIT V: Advanced Topic
Micro and smart system based switches for RF and Microwave applications, inductors and capacitors, RF filters, phase shifters, transmission lines and components, antenna, integration and packaging.

Text Books:
[1] MEMS & Microsystems: Design and Manufacture, Tai-Ran Tsu, Tata Mc-Graw-Hill.
[2] RF MEMS and their applications, V.Varadan, K. J. Vinoy, K.A. Jose, Wiley.

References:
[1] Microsystems Design, S. D. Senturia, Kluwer Academic Publishers, 2001.
[2] Analysis and Design Principles of MEMS Devices, Minhang Bao, Elsevier
[3] Design and Development Methodologies, Smart Material Systems and MEMS: V. Varadan, K. J. Vinoy, S. Gopalakrishnan, Wiley.
[4]MEMS- Nitaigour Premchand Mahalik, TMH 2007

ADVANCES IN VLSI DESIGN			
Course Code:	**EC669**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**
MODERN OPTIMIZATION TECHNIQUES			

UNIT I: Introduction
MOS and CMOS static plots, switches, comparison between CMOS and BI - CMOS.MESFET and MODFET operations, quantitative description of MESFETS.MIS systems in equilibrium, under bias, small signal operation of MESFETS and MOSFETS.

UNIT II: Short channel effects and challenges to CMOS: Short channel effects, scaling theory, processing challenges to further CMOS miniaturization

UNIT III: Beyond CMOS
Evolutionary advances beyond CMOS, carbon Nano tubes, conventional vs. tactile computing, computing, molecular and biological computing Mole electronics-molecular Diode and diode- diode logic. Defect tolerant computing.

UNIT IV : Super buffers, Bi-CMOS and Steering Logic
Introduction, RC delay lines, super buffers- An NMOS super buffer, tri state super buffer and pad drivers, CMOS super buffers, Dynamic ratio less inverters, large capacitive loads, pass logic, designing of transistor logic, General functional blocks - NMOS and CMOS functional blocks.

UNIT V: Special circuit layouts & technology mapping and System Design
Introduction, Talley circuits, NAND-NAND, NOR- NOR, and AOI Logic, NMOS, CMOS Multiplexers, Barrel shifter, Wire routing and module lay out. CMOS design methods, structured design methods, Strategies encompassing hierarchy, regularity, modularity & locality, CMOS Chip design Options, programmable logic, Programmable inter connect, programmable structure, Gate arrays standard cell approach, Full custom Design.

Text Books:
[1] Kevin F Brrnnan Introduction to semi conductor device, Cambridge Publications
[2] Eugene D Fabricius Introduction to VLSI design, McGraw-Hill International Publications

References:
[1] D.A Pucknell Basic VLSI design, PHI Publication
[2] Wayne Wolf, Modern VLSI Design Pearson Education, Second Edition, 2002

Course Code:	EC671	Credits:	3
No. of Lectures (Hrs/Week):	3	Mid Sem Exam Hours:	2
VLSI-RELIABILTY ENGINEERING			

UNIT I: Artificial Neural Networks (ANN)
Objectives-History-Biological inspiration, Neuron model, Single input neuron, Multi-input neuron, Network architecture, Single layer of neurons, Multi-layers of Neurons.

UNIT II: Perceptron and Learning
Perceptron architecture, Stingle-neuron perceptron, Multi-neuron perceptron- Perceptron Learning Rule, Constructing learning rules, Training multiple neuron perceptrons. Associative Learning: Simple associative network, Unsupervised Hebbrule- Hebb rule with decay, Instar rule, Kohonen rule. Widro-Hoff Learning: Adaline Network, Single Adaline, Mean square Error, LMS algorithm, Analysis of Convergence.

UNIT III: Neural Network Roles in VLSI Design
Applications of Artificial Neural Networks to Function Approximation, Regression, Time Series and Forecasting.

UNIT IV: Genetic Algorithms and its Mathematical Foundations
Introduction, robustness of traditional optimization and search methods, goals of optimization, difference between genetic algorithms and traditional methods, a simple genetic algorithm, hand simulation, Grist for the search mill, similarity templates, learning the lingo. Foundation theorem, schema processing, the two armed and k-armed bandit problem, schemata processing, building block hypothesis, minimal deceptive problem (MDP), extended schema analysis, MDP results, similarity templates as hyper planes.

UNIT V: Advanced Topics
Data structures, reproduction, crossover and mutation, a time to reproduce and a time to cross, main program and results, mapping objective functions to fitness form, fitness scaling, codings, a multiparameter mapped fixed point coding, discretization, constraints.

Text Books:

[1] Neural Network Design, PWS publishing company, 1995.
[2] Introduction to Artificial Neural Systems, Jaico Pub.House, Bombay, 1994.
[3] Neural Computing : Theory and practice, Van Nastrand Reinhold, 1989.

References

[1] Haykin S., Neural Networks-A Comprehensive Foundations, Prentice-Hall International, New Jersey, 1999.
[2] Freeman J.A., D.M. Skapura, Neural Networks: Algorithms, Applications and Programming Techniques, Addison-Wesley, Reading, Mass, (1992).
[3] Golden R.M., Mathematical Methods for Neural Network Analysis and Design, MIT Press, Cambridge, MA, 1996.

Course Code:	**EC673**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Probability Plotting and Load- Strength Interference
Statistical distribution , statistical confidence and hypothesis testing, probability plotting techniques – Weibull, extreme value, hazard, binomial data; Analysis of load – strength interference , Safety margin and loading roughness on reliability.

UNIT II: Reliability Prediction, Modeling and Design
Statistical design of experiments and analysis of variance Taguchi method, Reliability prediction, Reliability modeling, Block diagram and Fault tree Analysis ,petric Nets, State space Analysis, Monte carlo simulation, Design analysis methods – quality function deployment, load strength analysis, failure modes, effects and criticality analysis.

UNIT III: Electronics and Software System Reliability
Reliability of electronic components, component types and failure mechanisms, Electronic system reliability prediction, Reliability in electronic system design; software errors, software structure and modularity, fault tolerance, software reliability, prediction and measurement, hardware/software interfaces.

UNIT IV: Reliability Testing and Analysis
Test environments, testing for reliability and durability, failure reporting, Pareto analysis, Accelerated test data analysis, CUSUM charts, Exploratory data analysis and proportional hazards modeling, reliability demonstration, reliability growth monitoring.

UNIT V Manufacture and Reliability Management
Control of production variability, Acceptance sampling, Quality control and stress screening, Production failure reporting; preventive maintenance strategy, Maintenance schedules, Design for maintainability, Integrated reliability programs, reliability and costs, standard for reliability, quality and safety, specifying reliability, organization for reliability.

Text Books:
[1] Patrick D.T. O'Connor, David Newton and Richard Bromley, Practical Reliability Engineering, Fourth edition, John Wiley & Sons, 2002
[2] David J. Klinger, Yoshinao Nakada and Maria A. Menendez, Von Nostrand Reinhold, New York, AT & T Reliability Manual, 5th Edition, 1998.

Reference:
[1] Gregg K. Hobbs, Accelerated Reliability Engineering - HALT and HASS, John Wiley & Sons, New York, 2000.

SENSOR NETWORKS			
Course Code:	**EC647**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Sensor Network Operations
Overview of mission-oriented sensor networks, trends in sensor development, mission oriented sensor networks, dynamic systems perspective, Dense sensor networks, robust sensor positioning in wireless ad hoc sensor networks, trigonometric k clustering (TKC) for censored distance estimation, sensing coverage and breach paths in surveillance wireless sensor networks.

UNIT II: Lower Layer Issues-MAC, Scheduling, and Transmission
Medium access control for sensor networks, comprehensive performance study of IEEE 802.15.4, providing energy efficiency for wireless sensor networks, link adaptation techniques.

UNIT III: Network Routing
Load balanced query protocols for wireless sensor networks, energy efficient and MAC aware routing for data aggregation in sensor networks, ESS low energy security solution for large-scale sensor networks based on tree ripple zone routing scheme.

UNIT IV: Sensor Network Applications
Evader centric program, Pursuer centric program, hybrid pursuer evader program, efficient version of hybrid program, Implementation and simulation results

UNIT V: Embedded Soft Sensing for Anomaly Detection
Mobile robot simulation setup, software anomalies in mobile robotic networks, soft sensor, software anomaly detection architecture, anomaly detection mechanisms, test bed for software anomaly detection in mobile robot application, multisensor network-based framework; Basic model of distributed multi sensor surveillance system, super resolution imaging, optical flow computation, super resolution image reconstruction, experimental results.

Text Books:
[1] Sensor Network Operations, Shashi Phoha, Thomas F. La Porta , Chrisher Griffin, Wiley-IEEE Press March 2006.
[2] Wireless sensor networks, Jr. Edger H. Callaway, CRC Press.

References:
[1] Wireless Sensor Networks, I. F. Akyildiz and M. C. Vuran, John Wiley and Sons Publ. Company
[2] Wireless Sensor Networks: An Information Processing Approach, Feng Zho, Morgan Kaufmann

MIXED SIGNAL VLSI DESIGN			
Course Code:	**EC519/EC675**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: Signals, Filters, and Tools
Sinusoidal Signals, Pendulum Analogy, Amplitude in the x-y Plane, In-Phase and Quadrature Signals, Complex (z-) Plane, Comb Filters, Digital Comb Filter, Digital Differentiator, Intuitive Discussion of the z-Plane, Comb Filters with Multiple Delay Elements, Digital Integrator, Delaying Integrator, Exponential Fourier Series, Fourier Transform, Dirac Delta Function .

Unit II: Sampling and Aliasing
Sampling, Impulse Sampling, Time Domain Description of Reconstruction, Decimation, Sample-and-Hold, S/H Spectral Response, Reconstruction Filter, Circuit Concerns for Implementing the S/H, Track-and-Hold (T/H), Interpolation, Zero Padding, Hold Register, Linear Interpolation, K-Path Sampling, Switched-Capacitor Circuits, Non-Overlapping Clock Generation, Circuits Implementing the S/H, Finite Op-Amp Gain-Bandwidth, Auto zeroing,

Unit III: Analog Filters
Integrator Building Blocks, Lowpass Filters, Active-RC Integrators, Effects of Finite Op-Amp Gain Bandwidth Product, Active-RC SNR, MOSFET-C Integrators, gm-C Integrators, Common-Mode Feedback Considerations, High-Frequency Transconductor, Discrete-Time Integrators, Frequency Response of an Ideal Discrete-Time Filter, Filtering Topologies, Bilinear Transfer Function, Active-RC Implementation, Transconductor-C Implementation.

Unit IV: Digital Filters
Models for DACs and ADCs, Ideal DAC, Modeling of Ideal DAC, Ideal ADC, Number Representation, Increasing Word Size, Adding Numbers and Overflow, Two's Complement Sinc-Shaped Digital Filters, Counter, Aliasing, Accumulate-and-Dump, Lowpass Sinc Filters, Averaging without Decimation, Cascading Sinc Filters, Finite and Infinite Impulse Response Filters, Bandpass and Highpass Sinc Filters, Frequency Sampling Filters.

Unit V: Data Converter SNR
Quantization Noise, Quantization Noise Spectrum, Bennett's Criteria, RMS Quantization Noise Voltage, Quantization Noise as a Random Variable, Quantization Noise Voltage Spectral Density, Power Spectral Density, SNR, Effective Number of Bits, Coherent Sampling, SNDR, Spurious Free Dynamic Range, Dynamic Range, Specifying SNR and SNDR, Clock Jitter.

Text Books:
[1] Jacob Baker, CMOS Mixed Signal Circuit Design, TMH

References:
[1] Yannis Tsividis ,"Mixed Analog-Digital VLSI Device and Technology", Wiley
[2] Roubik Gregorian ,"Introduction to CMOS Opamps and Comparators",TM

ADVANCED DIGITAL VLSI DESIGN

DSP INTEGRATED CIRCUITS			
Course Code:	**EC521/EC677**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

Unit I: DSP Integrated Circuits and VLSI Circuit Technologies
Standard digital signal processors, Application specific IC's for DSP, DSP systems, DSP system design, Integrated circuit design. MOS transistors, MOS logic, VLSI process technologies, Trends in CMOS technologies.

Unit II: Digital Signal Processing
Digital signal processing, Sampling of analog signals, Selection of sample frequency, Signal- processing systems, Frequency response, Transfer functions, Signal flow graphs, Filter structures, Adaptive DSP algorithms, DFT-The Discrete Fourier Transform, FFT-The Fast Fourier Transform Algorithm, Image coding, Discrete cosine transforms.

Unit III: Digital Filters and Finite Word length Effects
FIR filters, FIR filter structures, FIR chips, IIR filters, Specifications of IIR filters, Mapping of analog transfer functions, Mapping of analog filter structures, Multirate systems, Interpolation with an integer factor L, Sampling rate change with a ratio L/M, Multirate filters. Finite word length effects -Parasitic oscillations, Scaling of signal levels, Round-off noise, Measuring round-off noise, Coefficient sensitivity, Sensitivity and noise.

Unit IV: DSP Architectures and Synthesis of DSP Architectures
DSP system architectures, Standard DSP architecture, Ideal DSP architectures, Multiprocessors and multicomputers, Systolic and Wave front arrays, Shared memory architectures. Mapping of DSP algorithms onto hardware, Implementation based on complex PEs, Shared memory architecture with Bit – serial PEs.

Unit V: Arithmetic Units and Integrated Circuit Design
Conventional number system, Redundant Number system, Residue Number System, Bit-parallel and Bit-Serial arithmetic, Basic shift accumulator, Reducing the memory size, Complex multipliers, Improved shift-accumulator. Layout of VLSI circuits, FFT processor, DCT processor and Interpolator as case studies. Cordic algorithm.

Text Books:
[1] Lars Wanhammer, "DSP Integrated Circuits", 1999 Academic press, New York
[2] A.V.Oppenheim et.al, "Discrete-time Signal Processing", Pearson Education, 2000.

References:
[1] Emmanuel C. Ifeachor, Barrie W. Jervis, " Digital signal processing – A practical approach", Second Edition, Pearson Education, Asia.
[2] Keshab K.Parhi, "VLSI Digital Signal Processing Systems design and Implementation", John Wiley & Sons, 1999.

Course Code:	EC679	Credits:	3
No. of Lectures (Hrs/Week):	3	Mid Sem Exam Hours:	2
TEST AND VERIFICATION OF VLSI CIRCUITS			

UNIT I: Introduction
Basic principle of MOSFETs, Introduction to large signal MOS models (long channel) for digital design. The MOS Inverters: Static and Dynamic characteristics: Inverter principle, Depletion and enhancement load inverters, the basic CMOS inverter, transfer characteristics, logic threshold, Noise margins, and Dynamic behavior, transition time, Propagation Delay, Power Consumption.

UNIT II: MOS Circuit Layout & Simulation
Layout design rules, MOS device layout: Transistor layout, Inverter layout, CMOS digital circuits layout & simulation, Circuit Compaction; Circuit extraction and post-layout simulation.

UNIT III: Combinational MOS Logic Design
Static MOS design: Complementary MOS, Ratioed logic, Pass Transistor logic, complex logic circuits, DSL, DCVSL, Transmission gate logic. Dynamic MOS design: Dynamic logic families and performances. Memory Design: ROM & RAM cells design

UNIT IV: Sequential MOS Logic Design
Static latches, Flip flops & Registers, Dynamic Latches & Registers, CMOS Schmitt trigger, Monostable sequential Circuits, Astable Circuits. Adders, Multiplier Circuits.

UNIT V: Interconnects & IO Buffers and BiCMOS Logic Circuits
Interconnect delays, Cross Talks. Introduction to low power design, Input and Output Interface circuits. BiCMOS Logic Circuits: Introduction, Basic BiCMOS Circuit behavior, Switching Delay in BiCMOS Logic circuits.

Text Books:
[1] Kang & Leblebigi CMOS Digital IC Circuit Analysis & Design- McGraw Hill, 2003
[2] J.M. Rabey, Digital Integrated Circuits Design, Pearson Education, Second Edition, 2003
[3] Weste and Eshraghian, Principles of CMOS VLSI design Addison-Wesley, 2002

Reference:
[1] W Wolf Modern VLSI Design.
[2] David A. Hodges, Horace G. Jackson, Resve Saleh, Analysis & Design of Digital Integrated Circuits, 3rd Edi Mc Graw Hill, 2003.

Course Code:	**EC681**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

EM INTERFERENCE AND CAPABILITIES IN SYSTEM DESIGN

UNIT I: Introduction

Basic Concepts, Functional Modeling: Truth table and primitive cubes, Binary decision diagrams, Basic RTL constructs, Timing Modelling, Structural Modeling: External Representations Structural Properties, Internal representations, Wired Logic and bidirectionality.

UNIT II: Logic Simulation

Types of simulations, The unknown logic values, Complied simulation, Event driven simulation Delay Models for gates, Element Evaluation, Hazard Detection, Tristate Logic, MOS Logic, other delay models: Rise and Fall Delays, Inertial Delays, Ambiguous Delays, Oscillation Control.

UNIT III: Fault Modeling and Simulation

Logical Fault Models, Fault Detection and Redundancy: Combinational Circuits, Sequential Circuits, Fault Equivalence and Fault location: Combinational Circuits, Sequential Circuits, Fault Dominance, Single stuck Fault model, Multiple stuck at Fault model, General Fault Simulation Techniques: Serial Fault, Parallel Fault, Deductive Fault, Concurrent Fault, Fault Simulation for Combinational Circuits.

UNIT IV: Testing for Faults

Basic Issues, ATG for SSFs in Combinational Circuits: Fault Oriented ATG, Common Concepts, Algorithms, Selection Criteria, Fault Independent ATG, Random Test Generation, Combined Deterministic/Random Test Generation, ATG for single stuck at faults in sequential Circuits, Bridging Fault model, Detection of feedback and non feedback Bridging Faults.

UNIT V: Design for Testability

Testability: Tradeoffs, Controllability and Observability, Ad Hoc Design for Testability Techniques: Test points, Initialization, Monostable multivibarators, Oscillators and Clocks, Controllability and Observability by means of scan registers, Generic scan based designs.

Text Books:

[1] Digital Systems Testing & Testable Design, Miron Abramovici, Melvin A. Breuer, Arthur D. Friedman.
[2] An Introduction to Logic Circuit Testing, Parag K Lala

REFERENCE BOOKS

[1] VLSI Test Principles and Architectures: Design for Testability (Systems on Silicon), Laung-Terng Wang, Cheng-Wen Wu, Xiaoqing Wen.

ALGORITHM FOR VLSI DESIGN AUTOMATION			
Course Code:	EC685	Credits:	3
Course Code:	EC683	Credits:	3
No. of Lectures (Hrs/Week):	3	Mid Sem Exam Hours:	2
No. of Lectures (Hrs/Week):	3	Mid Sem Exam Hours:	2
Total No. of Lectures:	45	End Sem Exam Hours:	3
Total No. of Lectures:	45	End Sem Exam Hours:	3

UNIT I: Basic EMC concepts at IC level

Introduction , Definition of EMC, EMI, EMS and EME, Sources of electromagnetic interference, Electromagnetism versus integrated circuit design, Electrical length, Near field versus far field, Radiation of a conductor , Basic EMC antenna concepts, Radiated, induced and conducted disturbances, Practical example, Intra-chip versus externally-coupled EMC, EMC in automotive applications.

UNIT II: EMC of Integrated Circuits and Distortion

Relationship between EMI resisting design and distortion , Linear distortion, Nonlinear distortion (rectification) , Weak and strong nonlinear distortion, diode connected NMOS transistor , NMOS source follower, NMOS current mirror, Capacitor decoupling the mirror node, Low-pass *R-C* filter in the mirror node , EMI resisting (4-transistor) current mirror , EMI resisting (Wilson totem pole) current mirror , Comparison of EMI susceptibility of current mirrors , EMI susceptibility in ESD protections.

UNIT III: EMI Resisting Analog output circuits

Categorization of analog output structures, Common-drain output circuits, Common-source output circuits, Comparing the electromagnetic susceptibility, Large EMI amplitudes, EMI resisting DC current regulator , EMI issues in a classic DC current regulator, EMI issues: small signal analysis large signal analysis, Decoupling capacitor *Cd* , DC current regulator with a high immunity to EMI Measurements.

UNIT IV: EMI Resisting Analog input circuits

Electromagnetic immunity of CMOS operational amplifiers, Asymmetric slew rate, Strong nonlinear behaviour of the input differential pair, Weak nonlinear behaviour of the input differential pair, EMI induced offset in a classic differential pair , Classic differential pair using source degeneration, Cross-coupled differential pair, Differential pair with low-pass *R-C* filter, Improved cross-coupled differential pair, Source-buffered differential pair, Comparison, EMI induced offset measurement setups, Measurements.

UNIT V: Advance Topics

CMOS bandgap voltage references with a high immunity to EMI, EMI injection in a bandgap reference, Small signal analysis, Large signal analysis, EMI resisting bandgap reference , Small signal analysis , Large signal analysis, EMI resisting bandgap reference, Small signal analysis, Large signal analysis, Startup circuit and biasing, Measurements.

Text Books:

[1] EMC of Analog Integrated Circuits, Jean-Michel Redoute, Michiel Steyaert

References:

[1] Electromagnetic compatibility of integrated circuits: techniques for low emissions and susceptibility, Sonia Ben Dhia, Mohamed Ramdani, Étienne Sicard.
[2] Electromagnetic Compatibility Engineering , Henry Ott.

UNIT I: Introduction

Architectural Design , Logic Design, Physical Design , Full-custom Layout**,** Gate-array Layout, Standard-cell Layout Macro-cell Layout, Programmable Logic Arrays, FPGA layout**,** Difficulties in Physical

Design, Problem Subdivision, Computational Complexity of Layout Subproblems, Solution Quality, Nets and Netlists, Connectivity Information, Weighted Nets, Grids, Trees, and Distances.

UNIT II: Circuit Partitioning and Floorplanning
Cost Function and Constraints: Bounded Size Partitions, Minimize External Wiring, Approaches to Partitioning Problem: Kernighan-Lin Algorithm, Variations of Kernighan-Lin Algorithm, Fiduccia Mattheyses Heuristic, Simulated Annealing, Floorplanning Model, Approaches to Floorplanning, Cluster Growth ,Simulated Annealing ,Analytical Technique , Dual Graph Technique.

UNIT III: Placement
Complexity of Placement , Problem Definition , Cost Functions and Constraints: Estimation of Wirelength, Minimize Total Wirelength , Minimize Maximum Cut , Minimize Maximum Density, Maximize Performance, Other Constraints, Approaches to Placement: Partition-Based Methods, Limitation of the Min-cut Heuristic, Simulated Annealing , Numerical Techniques.

UNIT IV: Routing
Problem Definition, Cost Functions and Constraints: Placement Constraints , Number of Routing Layers Geometrical Constraints, Maze Routing Algorithms: Lee Algorithm, Limitations of Lee Algorithm for Large Circuits ,Connecting Multi-point Nets ,Finding More Desirable Paths, Further Speed Improvements, Line Search Algorithms, Other Issues: Multi Layer Routing , Ordering of Nets , Rip-up and Rerouting, Power and Ground Routing.

UNIT V: Advanced Topics
Cost Functions and Constraints , Routing Regions: Routing Regions Definition, Routing Regions Representation, Sequential global Routing: The Steiner Bee Problem, Global Routing by Maze Running, Integer Programming ,Global Routing by Simulated Annealing : The First Stage , The Second stage, Hierarchical Global Routing.

Text Books:
[1] VLSI physical design automation: theory and practice, By Sadiq M. Sait, Habib Youssef.
[2] Algorithm for VLSI physical design automation by Naveed A. Sherwani.

References:
[1] Essential Electronic Design Automation (EDA), Mark D Birnbaum.
[2] Physical Design Automation for VLSI systems, Bryan D Ackland.
[3] Practical Problems in VLSI Physical Design Automation, Sung Ku Lim.

SMART ANTENNA SYSTEMS			
Course Code:	**EC643**	**Credits:**	**3**
No. of Lectures (Hrs/Week):	**3**	**Mid Sem Exam Hours:**	**2**
Total No. of Lectures:	**45**	**End Sem Exam Hours:**	**3**

UNIT I: Basic Concepts of Radiation
Radiation mechanism: Basic sources of Radiation- Current distribution on antennas, Basic antenna parameters.

UNIT II- Analysis and Synthesis of Antennas
Vector potential, Antenna theorems and definitions, dipole, loop, reflector, slot antennas. Types of linear arrays, current distribution in linear arrays, Antenna array synthesis techniques.

UNIT III Smart Antennas
Spatial processing for wireless systems: Introduction, Vector channel impulse response & the spatial signature. Spatial processing receivers, fixed beam forming Networks, switched beam systems, Adaptive antenna systems, Wide band smart antennas, Digital radio receiver & software radio for smart antennas.

UNIT IV- Smart Antenna Techniques for CDMA
Non-coherent & coherent CDMA spatial processors, spatial processing rake receiver, Multi-user spatial processing, dynamic resectoring, down link beam forming for CDMA, MIMO.

UNIT V: Microstrip Antenna
Radiation Mechanism and Excitation techniques : Microstrip dipole; Patch ,Rectangular patch, Circular patch, and Ring antenna – radiation analysis from cavity model; input impedance of rectangular and circular patch antenna; Microstrip array and feed network; Application of microstrip array antenna.

Text Books:
[1] Balanis A., Antenna Theory Analysis and Design, John Wiley and Sons, New York, 1982.
[2] Joseph C. Liberti, Theodore S. Rappaport – Smart Antennas for Wireless Communications: IS95 and third generation CDMA Applications, Prentice Hall, Communications Engineering and Emerging Technologies Series.

References:
[3] I.J. Bahl and P. Bhartia, Microstrip Antennas,Artech House,Inc.,1980
[4] W.L.Stutzman and G.A.Thiele,Antenna Theory and Design, 2nd edition,John Wiley& Sons Inc.,1998.